Theory of Operation

The Sienna HF transceiver is organized into five major blocks:

- DC Power conditioning (DCD board)
- Control (Controller, Front Panel and VFD boards)
- Receiver (Receiver, BPF and IF Filter boards)
- Transmitter (Transmitter, TXBPF, Tuner and 100W amplifier boards)
- PC (PCPS and PC boards)

Refer to the Block Diagram on page 43 and the Schematics starting on page 44.

DC Power Conditioning: DCD board

Over-voltage. Under-voltage, reverse polarity and overcurrent protection

Kit rigs sometimes fail to do some basic power conditioning on the input, making them failure-prone. The Sienna includes over- and under-voltage protection, over-current protection (fuses), and reverse polarity protection. In addition, the internal DC voltages of +5V, +9V and –9V are derived from regulators which have additional input and output protection circuitry.

Refer to the DCD board, sheet 3. The DC input from Anderson Powerpole connectors is protected from reverse polarity by diode D6. Capacitor C21 adds some protection against static discharge and shunts any high frequency energy to ground.

R26 and zener diode D9 tap a small amount of current from the input even when power is off in order to provide a 2.7V DC reference for comparator U7, an LM393. Capacitor C22 assures that any rapid changes in the input voltage will be swamped out, keeping the reference voltage stable until the input voltage drops well below normal.

R9, R10, D7 and C20 provide a voltage divider with long attack and very fast decay, setting the low trip point at about 1/3 of the input voltage. When the voltage rises above 2.7*3 (8.4V), the output of comparator U7 (pin 1) goes high. As long as the other comparator output (pin 7) is not low, the DC voltage will be enabled. Diode D7 assures that when the voltage drops, capacitor C20 is discharged quickly.

R24, R25 and C23 form a similar divider and stabilizer to detect when the voltage is above 15V.

Resistors R11 and R12 on one comparator, and R13 and R23 on the other, add a couple of Volts of hysteresis to keep the output of the comparators from oscillating at the trip points.

If the output of either comparator goes low, transistor Q2 turns off , causing K19, a 25A auto-

motive relay, to open, which removes power. When the comparator outputs are both high, pullup resistor R14 assures that Q2 will be on, enabling the relay to turn on. The relay cannot actually turn on unless the on/off switch is pushed because one side of the relay coil is routed through the switch to DC power.

Fuse F1 protects the radio from overcurrent conditions. This is a 9A Resettable fuse. When it warms up enough due to overcurrent conditions, it suddenly develops a high resistance, keeping high current from flowing. As it cools, it automatically resets.

When Q2 and the on/off switch are on, DC voltage appears at pad W3, which provides power for the 100W amplifier. Since this is a high current lead, it is located as close as possible to the relay to minimize voltage drop. A short cable connects this point to the amp. When the tray is rotated up for service, an extension cable is required. This extension cable will have noticeable voltage drop when the 100W amp is in use, so performance could suffer. As a result, it should not be used except for testing.

On/off switch LED

Comparator U6 is used to detect when the DC voltage going to the regulators has dropped to a low enough level that they are about to shut down. When the voltage gets to a little over 10V, the LED inside the on/off switch is turned from green to red. This is useful when operating the radio from batteries.

Regulators

The 5V regulator, U8, is a low-drop-out regulator, which means that it does not require much more voltage going in than it generates. However, excessive voltage going in would make it run very hot, so its input voltage is dropped by pass transistor Q1 and regulator U9 from the input of 11V-15V. Both regulators have input and output protection. They are mounted to the tray, providing excellent heatsinking, and the dual fans in the compartment below the tray help keep the tray cool during normal operation. During service, with the top open, the cooling effect of the fans is greatly reduced, and the tray can get quite hot. Operation with the top off is not recommended for long periods of time.

U10 is a MAX765 negative voltage generator. It is a “chopper”, which turns the DC input voltage into an AC voltage which is then converted back to DC and output as a negative DC voltage. This negative voltage is used by the receiver to allow high performance dual supply opamps to be used. RFC1 helps keep the switching transients off the line, which could induce noise into the sensitive receiver circuits.

The raw DC input is also fed to the receiver, controller and transmitter. The receiver uses the

raw input voltage on the audio output amplifiers in order to allow them to handle the very high instantaneous currents (up to an amp!) needed for good speech reproduction.

Antenna switch, SWR meter

The DCD board also has an antenna A/B switch and an SWR meter on it (see sheet 2 of 3 on the DCD/Tuner schematic). Relay K17 and K18 switch between main antennas A and B. The use of two relays instead of one provides better port-to-port isolation. A portion of the transmitted signal, both forward and reflected signals, is picked up by transformer T1 and fed into buffer U5. The outputs are clamped to keep the levels from exceeding 5V, and are fed to the main controller's A/D converters for measurement. C17, RV1 and RV2 are used to calibrate the meter so that the measured voltages correspond to correct power levels as measured against an external wattmeter. If no wattmeter is available, a 50 ohm dummy load allows the meter calibration to come close.

In order to handle both 10W transmitters and 100W amplifiers, the output of U5 is scaled by resistive dividers R5/R32 and R6/R33. A signal (/NOPA) from the amplifier goes high if the amplifier is present and enabled. If it is not present, R31 keeps the voltage low, forcing Q6 and Q7 to be off and removing the scaling factor.

Control circuits are discussed in the Controller theory section.

Control: Controller, Front Panel and VFD Boards

The main Controller board is the heart of the Sienna. An Atmel Mega644P microcontroller (U9) running at a clock frequency of 16MHz provides the main control functions, and a second Mega644P (U30) is used for Keyer, VOX/AntiVOX detection, microphone sampling in FM, keypad detection and meter backlight functions. A +/-1 PPM Temperature Compensated Crystal Oscillator (TCXO), six Direct Digital Synthesis (DDS) chips and associated bandpass filters and high bandwidth buffer/amplifiers provide a clean source of high purity, low phase noise local oscillators for the transmitter and receiver.

Refer to the Controller schematic pages, Sheets 1 through 11. While this four layer board is very dense and may look formidable, the circuitry is actually very straightforward. Sheet 1 shows the DC input conditioning. Two 3.3V regulators are used to drop the 5V down to 3.3V for the DDS chips and the buffers that drive their data and address busses. R2/C3 and R38/C46 provide decoupling for the analog 5V supply that is used for the A/D converter circuits on the microprocessors.

Main microprocessor

Sheet 2 shows the main microprocessor. This processor has 64K bytes of internal program storage, 4K bytes of RAM and 2K bytes of Electrically Erasable Programmable Read-Only Memory (EEPROM). The EEPROM stores constants and lookup tables such as the filter parameters, current state of the instrument, band plans and so on. A software timer writes data to the EEPROM every 10 seconds if anything that needs to be saved has changed. Main memory and EEPROM memory can be rewritten through the SPI bus (J6), which is what is used at the factory to initially program the processor, or through the RS-232C port (pins 9 and 10 on the processor, going to U7 on Sheet 4. The ST207E converts CMOS voltages into RS-232C levels which are fed to the PC or the back panel via J4. Other RS-232C control lines (RTS, CTS) are also converted to CMOS levels by U7 and fed to the secondary microprocessor to allow handshake control and use of RTS as a CW key. RS-232C signal DTR is fed into the PTT circuitry via Q2 and Q4. Q21 allows this signal to be disabled (via control bit SERDIS), since at boot-up, the PC can pull the DTR line and we do not want it causing the rig to go into transmit mode!

U8 is a power-on reset chip providing a long reset pulse to start the processor correctly when power is first applied.

PTT

PTT stands for Push-to-Talk and is normally associated with a pin on the microphone. The Sienna, however, defines the internal transmitter on/off control line as PTT. When the signal is low true (0V), it is named LPTT. The inverted version of that is HPTT. The microphone control input is referred to as simply PTT. In the following discussion, unless stated explicitly as referring to the microphone control line, PTT is used generically to mean the line that controls the transmitter.

PTT control lines are shown on Sheet 4: Q7 and Q5 buffer the microphone's PTT line, and Q10

allows the processor to override it (PTTO).Q1 allows the Keyer microprocessor to take control of the internal PTT line (PTT_Keyer) so that it can provide time delays before and after a keying signal in order not to chop off the beginning or end of the RF keying waveform, and to provide the desired full– and semi-break-in delays needed.

Sheet 4 also shows the 5V to 3.3V level converter (U10) that drives address and data lines on the DDS chips.

A-to-D (A/D) Converters

Going back to Sheet 2, the Mega644P has eight A/D converter inputs. There is actually only one 10-bit A/D inside the chip, and it uses a multiplexer to look at one analog input at a time. The signals fed into the first seven inputs are the FM squelch, AF Gain, RF Gain, Mic Gain, Headphone Volume, RF Power and RF Processor pots that are located on the Front Panel board and fed into the Controller on J9 (Sheet 6). The eighth analog input comes from U19 on Sheet 7. This CMOS analog multiplexer selects one of eight additional voltages: Forward and Reflected Power from the DCD/Tuner board; Supply voltage, ALC/compression and Driver Current from the 10W transmitter board; Final Current from the 100W PA board, S-Meter value from the Receiver board, and the value of the IF Filter switch on the Front Panel. An interrupt routine in the microprocessor selects and samples one of these 15 voltages every time an A/D conversion completes (about every 100 microseconds).

Parallel Data Bus

Also on Sheet 2, Port C of the processor is used as an 8-bit parallel data bus for all boards. This bus is buffered by U15 to become the “XBus”. Its output is enabled only when data on one of the boards needs to be changed, otherwise pull-up resistors on each board terminate the bus and keep it quiet to avoid causing unnecessary digital interference to the transmitter or receiver.

U20 is an address decoder. AS0, AS1 and AS2 (U34, Sheet 6) select one of eight data strobe pulses for the DDS chips and read/write pulses to the Keyer microprocessor.

I/O Strobes, inter-processor communications and address decoding

Port B on the microprocessor is used for I/O control. IOStrobe1 and /IOStrobe2 serve as clock pulses to output data from Port C to the various I/O chips on the Controller board. (The “/” in front means that the signal is low true, meaning that it is normally high and pulses low when active.) DispRDY and /DispCk are signals from and to the Vacuum Fluorescent Display board that are fed to the Controller board from J17 on Sheet 7. KeyerRDY is a signal from the Keyer microprocessor (U30, pin 42, Sheet 3) that tells the main processor that data is either ready on port C or has been accepted from port C. Q12 provides a Frequency Update pulse for all DDS chips. A4 and A5 are address lines for the DDS chips.

Port D has the RS-232C data lines TXD and RXD, Rotary Pulse Generator (RPG) outputs from the two tuning dials, and additional address lines for the internal I/O ports and DDS chips.

Sheet 5 shows address decoding for the 16 data strobe lines /Strobe1 though /StrobeG. These are used to output and input ("strobe") data on port C to and from all boards in the rig as well as various control functions on the Controller board. Sheets 5 and 6 show most of the internal ports. /Strobe1 and /Strobe2 read switch data from the Front Panel board. /Strobe2 also reads the state of the internal PTT line so that the processor knows when an external device (microphone, etc.) has activated the Push-to-Talk. /Strobe4 (Sheet6) and /Strobe7 (Sheet 5) provide outputs that directly drive LEDs inside the pushbutton switches on the Front Panel board. / Strobe6 (Sheet 5) and /Strobe5 (Sheet 6) provide 16 outputs that are used for a variety of control functions.

/Strobe8 through /StrobeG are fed to the Receiver, Transmitter and Tuner boards along with the XBus to program those boards. (See Sheet 7).

Serial Bus

A serial bus is also fed to the Receiver and Transmitter boards. SCL (U13 pin 9) and SDA (U13 pin 12, as well as U12 pin 17) (Sheet 5) form a high speed I^2C bus that is used to control DACs and Digitally Controlled Potentiometers (DCPs) on the Receiver and Transmitter boards. This bus is quiescent (not active) unless changes are needed, which helps avoid digital interference to sensitive receiver and transmitter circuits.

DDS

Sheets 8 through 11 show the DDS chips, bandpass filters on each output, and buffer amplifiers. Normally, DDS chips only require low pass filters on their outputs. Sienna uses bandpass filters so as to provide a much more constant impedance across the frequencies they must output, which helps to keep the level constant without the need for complex AGC circuitry. These devices take five bytes (AD9851) or 6 bytes (AD9852) of digital data and convert it directly to a frequency. The 0-512mV output must be converted to +/-256mV, amplified, and filtered to remove harmonics and other spurious signals (spurs). Close in spurs cannot be removed, but are typically down at least 70dB. A +/-1PPM TCXO provides a stable, low phase-noise 30MHz reference oscillator for all six DDS's.

The TV (Transmit VFO, not television!) signal coming from the TXVFO DDS (U5) on Sheet 8 is routed to a pair of Hittite GaAsFET switches which are controlled by TXVFILT (Sheet 5, pin 2 of U13). These switches allow one of two low pass filters to be applied to the output of the TXVFO amplifier. The TXVFO covers the frequency range 12.5 to 40.4MHz, so a low pass filter tuned for, say, 41MHz, would allow harmonics from frequencies at the lower end of the range to pass though, so a dual range filter helps keep the output pure. The firmware performs the switch at a TXVFO frequency of 22MHz (operating frequency of approx 11.3MHz).

Note that a similar switch is not needed for the RXVFO, because it operates at a much higher frequency range of 70-100MHz. Any harmonics of 70MHz fall well outside the upper cutoff of the Butterworth bandpass filter (105MHz).

LED Backlight

Sheet 7 shows backlighting circuitry for the meters. Q13, Q14 and Q15, along with the associated resistors, form a 3-bit binary control, allowing up to 8 brightness levels. The control lines for these MOSFETs come from the Keyer processor. High intensity LEDs D1-D4 provide plenty of light for the two meters.

MIC Bias

A 9V bias for electret mics can be turned on and off via Q16 (Sheet 7). The MICBIAS control bit from U13, pin 19 on Sheet 5 is used for this.

Keyer microprocessor

Sheet 3 is a diagram of the Keyer processor. The keyer speed, dot weight, dash weight and pitch pots from the Front Panel board are fed into the first four A/D inputs on port A (ADC0-3), similar to those of the main processor. A/D input 4 (the 5th input) comes from the transmitter (routed through the receiver board) and is a buffered, uncompressed version of the microphone audio, level shifted so that it idles at 2.5V with a peak-to-peak AC voltage of up to 5V. For VOX detection, the processor takes a running average of the AC voltage and computes an RMS value that is tested against a trip threshold set by a menu option. (During FM transmit, all A/D inputs are disabled except the mic, so that rapid sampling of the audio can occur, with this information passed to the main microprocessor in order to re-program the DDS chip controlling the BFO in real-time.) Similarly, the buffered and level-shifted speaker output is fed into A/D input 7 to form the Antivox input. Another RMS calculation is done on this signal and used along with a menu item to adjust the trip point of the VOX input up or down. A/D input 5 is the external keypad input. Yaesu designed the FH-1 keypad as a set of 12 buttons with resistors in series with them such that 12 different DC voltages from 0 to 5V are produced. The firmware tests these voltages to determine which button has been pushed and sends this coded information over the internal inter-processor bus (port C on both processors, with KeyerRDY, /KeyerRd and /KeyerWr). The Keypad input from the back panel is routed to A/D input 5, which reads the 0V to 5V signal to determine which of 12 buttons was pushed.

Port B, bit 3 is used as a Pulse Width Modulated output signal whose frequency is determined by the Pitch pot. The output is filtered by an RLC network and routed to the Front Panel board where it goes through the Sidetone pot and back to J11 which then goes to the Receiver board's audio output stage. If no front panel is present, jumper JP2 (Sheet 7), assures that the Sidetone (at full volume) will make it to the receiver board.

The dot paddle and dash paddle inputs are filtered and fed to two edge-driven interrupt lines (port D, bits 2 and 3). The manual key input is fed to bit 0, where it is sampled continuously in the 1ms interrupt routine. Outputs from the Keyer are the PTT_Keyer line, which is routed to the controller to allow the Keyer to control the PTT line, and the Key line, which is routed to the transmitter.

The Keyer processor also has its own SPI bus for programming and a power-on reset chip. This processor is not programmable by the user. Any changes to its internal firmware must be done either by the factory or in the field through the use of an inexpensive Atmel programmer board (STK500).

Display board

The VFD board is a Noritake GU256x64C-3900 model that is programmed with ASCII control command sequences. It connects to port C as just another I/O device. DispRDY and /DispCk signals provide the handshaking. Jumper JP1 on the Keyer processor tells the main controller if a front panel is present. One of the effects of this is to cause the display routines to be ignored if no front panel is present.

Receiver: BPF, Receiver and IF Filter Boards

Refer to the block diagram on page xxx and to the schematics on pages xxx-xxx.

Antenna to bandpass filters

RF from the main antenna ports (A and B) passes through low pass filters and a transmit/ receive (T/R) PIN diode switch on the transmitter or 100W amplifier boards. From there, the signal enters the antenna input (J2) on the RXBPF board (See RXBPF schematic, Sheet 2). Relay K6 selects either this input or one from the Receive Antenna input (J3) after the latter is passed through a 35MHz low pass filter. The Receive Antenna does not pass through band-specific low pass filters or a T/R switch as does the main antenna, which reduces the loss, but also exposes it to potential intermodulation distortion (intermod) from strong shortwave stations. If you experience intermod when using the receive antenna, we recommend use of an external bandpass filter such as those made by Array Solutions. Back to back zener diodes on the Receive Antenna input protect against extremely strong signals.RFC1 is a 1mH choke that routes low frequencies to ground, reducing hum from power lines.

High-pass and bandpass filters, attenuator1, PSB™

The selected signal is then fed through a high-pass filter located between GaAsFET switches U5 and U6. This filter reduces the chance of intermod from strong AM broadcast stations and is engaged automatically when the receive frequency is above 1.6MHz. The signal then passes through a 10dB attenuator which can also be switched out. Pressing the front panel Pre2/Atten button activates this attenuator unless preamp1 is on. The output, “A” on the schematic, is then passed through eleven bandpass filters, each controlled by a pair of GaAsFET switches, with each filter handling a different segment of the HF spectrum. In addition, one pair of GaAsFETs (U20/U21 on Sheet 8 of the RXBPF board) is allocated as a bypass. This circuit represents the DZKit exclusive Passive Signal Boost (PSB)™. By skipping the BPFs, any associated front-end loss is eliminated at the expense of a potential increase in intermod, and an increase in the noise floor, since more spectrum is allowed in. However, on a fading band, that extra 5dB of “gain” (actually “lack of loss”) can spell the difference between hearing and not hearing a weak signal. PSB is not intended to be used except under such conditions. We do not recommend that you leave it enabled permanently even though signals will sound stronger.

Preamps, attenuator2

The selected bandpass filter’s output is point “B”. Referring to Sheet 9 on the RXBPF board, B

is routed directly to the first preamp (Q4 and associated circuitry) and to relay K4, where it can be fed to the RF output without preamps. The first preamp's output can be switched on by relay K1 and appears at point R2, which feeds preamp2 (Q4 and associated parts) and relay K5. If K5 is disabled, so is K2, and thus Q4 has no power and provides only a weak load for preamp1. If K2 and K5 are enabled, preamp1 is fed into preamp2 and then out to the RF output.

The preamps are low noise 2N5109 bipolar transistors set up for a power gain of about 12dB and coupled via broadband toroid transformers T1 and T2.

Receiver first IF

The final RF output of the BPF board feeds into the Receiver board at J14 (Sheet 2 of Rx Board). It is applied directly to a Minicircuits TUF-3 diode ring mixer (U6). Local oscillator LO1 from the controller, which is the VFO, is set to the displayed receive frequency plus 70.455MHz (or 70.000MHz if the 20kHz roofing filter is used) and fed into the LO port. The output, consisting of sum and difference frequencies and a number of other mixing products, splits into two paths via a 50 ohm resistive pad, with one leg driving an Inrad 4KHz bandpass filter at 70.455MHz and the other driving the FM receive and IF output circuitry.

The output of the bandpass filter is amplified by Q5, a dual-gate MOSFET with about 10dB of power gain. The second gate of Q5 is derived from the AGC circuitry on Sheet 6, buffered and inverted by U1 to provide a nominal 4V on gate 2, decreasing to 2V under full AGC action and reducing the gain accordingly. The source is biased at 1.9V, so the 4V on gate 2 represents 2.1V of gain enhancement. When the control voltage goes down to 2V in response to a strong signal detected by the 3rd IF, the differential of 0.1V reduces the gain to its minimum level. Diodes D11 and D12 provide temperature compensation while contributing to the source bias of 1.9V.

The output of Q5 feeds a Darlington transistor configuration, which provides high input impedance and low output impedance, necessary to successfully drive the next RF mixer. Resistors R101 and R126 set Q5's load impedance to about 2K ohms to provide a moderately high impedance load for the amplifier, whose nominal output impedance is about 200 ohms, while biasing the Darlington stage at a reasonable level. This preserves the power gain while allowing the stage to drive the low impedance (50 ohm) mixer load.

Receiver second IF

The 70MHz 1st IF output of the Darlington driver feeds U8, another TUF-3 mixer, along with LO2 from the controller set to 61.455Mhz (+/-, depending on filters in use and desired sideband). The difference product of about 9MHz is used for the 2nd IF, allowing a wide variety of Inrad crystal filters to be used. Transformer T4 boosts the 50 ohm output impedance of the mixer up to 1800 ohms while providing a factor of 6 voltage gain. The signal is fed into another amplifier (Q20, Sheet 3) that is identical to that of the previous stage. R54 and C51 decouple the buffered AGC voltage from the first stage.

Noise Blanker

The amplified 9MHz output of Q20 drives another Darlington buffer which then drives the

noise blanker circuitry on Sheet 4. The noise blanker is placed ahead of the crystal filters so that it can detect broadband noise pulses. The noise blanker is a simple 9MHz bandpass filter with an input and output impedance of about 120 ohms having a group delay of several microseconds, long enough for the IF amplifier, U12, to detect a signal and generate a blanking pulse just as the signal arrives at NBOUT. Three pulse widths are allowed using control bits NBPWA and NBPWB that are latched into U2 (Sheet 1). These bits are set by menu options. The NBOn-Off bit enables or disables the noise blanker by controlling whether power is applied to the detection circuit. When unpowered, the gating transistor, Q7, is always off. A DAC output, NBThr, provides a variable trip point, which is routed into Q8 by resistor R73. Note that NBThr is derived from the Squelch control. Since the FM receiver does not use the noise blanker, the same control is used for both circuits.

Since there is about 8dB of loss in the noise blanker, and up to 15dB of additional loss in the crystal filters and associated resistive pads, the output of the noise blanker is boosted by high bandwidth amplifier U25, an Analog Devices AD8000 op-amp in a gain of 11 configuration. The op-amp has high input impedance, allowing resistors R150 and R151 to set the input impedance to a value that matches the output impedance of the noise blanker, while providing enough gain to offset the loss in the noise blanker and crystal filters and a low output impedance capable of driving the crystal filters.

Crystal Filters

The crystal filters are plugged into 4 slots on the IF Filter board. Up to four filters can be installed on the IF Filter board at the 9MHz IF frequency. The first one is an Inrad 2311 6KHz filter. This provides enough bandwidth for AM reception. The standard filter is a 4-pole 2.4KHz Inrad model, providing good bandwidth for SSB and CW reception. All filters are switched via 1N914 diodes, and impedance matched on input and output via Minicircuits transformers and resistive pads (attenuators) . These pads serve several purposes. A portion of the pad is used to provide DC biasing for the diodes. They also serve to isolate the stages from each other and to help prevent downstream amplifier byproducts from feeding back into previous amplifiers, which would cause distortion. Finally, the presence of pads allows the attenuation to be tweaked so that the loss through the IF Filter board is about the same regardless of the loss characteristics of the various filters.

The crystal filters have various input/output impedances. The Inrad 2311 is about 400 ohms, whereas the others are 200 ohms, so an additional matching transformer is required as well as a different value pad.

The IF Filter board is designed to accommodate the filters (except the 2311) on Yaesu-compatible plug-in boards. A cutout in the bottom chassis provides access to these plug-in boards.

The Modewide control bit is set high in FM mode to de-select all filters and to turn on Q9 (Sheet 2) in order to provide a termination on the output side. Although the FM receiver follows a separate RF path that does not involve any of the circuitry discussed so far, the IF amplifiers do remain on, and this circuit helps keep them well-behaved during FM reception.

Receiver third IF

The filtered signal is brought back to the Receiver board via coaxial cable and immediately fed into an NXP SA612 Gilbert Cell mixer. This active mixer has about 10-12dB of low-noise gain and low input voltage requirements on the local oscillator (LO3). However, its input and output impedance is 1800 ohms, so a step up transformer is required on the input and a step-down transformer is required on the output. The third LO is set to 9.455MHz, so the primary mixing products are at about 18.455MHz and 455KHz. The output is immediately fed into the IF Filter board's 455KHz crystal and/or Collins mechanical filters, which rejects the 18.455MHz sum product and other secondary mixing products. An identical scheme is used for them as for the previously discussed 9MHz filters so they will not be re-hashed here.

AGC

The 455KHz filtered signal is brought back to the Receiver board via coaxial cable, where the 50 ohm impedance is transformed by T1 (Receiver board, Sheet 6) to 1800 ohms to drive the main IF amplifier (U9). This is the venerable MC1350, used in IF amplifiers in radio and TV for decades. Although no longer made by Motorola, it is still available from NTE. This amplifier has up to 50dB of power gain, and 60dB of AGC dynamic range. The AGC input on pin 5 provides dual slope AGC action that lends itself to direct observation on an S-meter, with 3.75-4.75V representing linear steps from S0 to S9, and 4.5V-5.5V representing a steeper scale for dB above S9.

The output of U9 is buffered by Q15 and fed to the final mixer. The emitter side of Q15 drives the AGC circuitry. As discussed earlier, Q6 provides a variable gain buffer based on which preamps are enabled. The output of Q6 drives a 10dB voltage gain amplifier with a frequency response optimized for 455KHz operation, whose output is rectified to produce a 0 to 120mV AGC control voltage (the cathode of D7). The output of D7 feeds a very long time constant filter (R70, C37) of about 22 seconds. This is the "IF-derived attack" of the AGC. Since this must drive an op-amp, the impedance must be low enough that the input offset and input bias current of the op-amp do not add a DC offset to the small AGC voltage. U27 (pins 1,2,3) multiplies the AGC voltage by 17 in a non-inverting configuration, resulting in a 0-2V output swing. The other half of U27 level shifts the 0-2V signal to 3.75-5.75V which becomes the AGC voltage that is fed into U9. U10 provides the necessary negative output that sets the differential amplifier offset. Because the LM358 is prone to a phenomenon known as "output inversion" if the input is allowed to go below –0.3V, a Schottky protection diode is used to keep that from happening. U10 receives its input from output "C" of a serially programmed D/A converter (U23, sheet 8). A calibration step involves setting this voltage so that the quiescent, no-signal AGC voltage is 3.75V and an S9 signal produces 4.75V.

The AGC output is level shifted back to 0-2V and used to drive the S-meter. Why not just take the 0-2V output out of U27? The answer is that the RFG control DAC is also used when the front panel RFG control is adjusted. By changing the RFG voltage, the AGC voltage at U27 pin 7 is forced to go up irrespective of what happens to the IF detection circuitry. We are used to seeing the S-meter rise when the RFG control is turned CCW, and if we just took the output of

U27 pin 1, this would not happen.

An AGCOff bit is used to short out the 0-120mV AGC control voltage, forcing the AGC voltage to stay at 3.75V and running the IF amplifier open loop at maximum gain.

The audio output prior to the volume controls is fed into U10 (pins 5,6,7) where it is amplified by a factor of 100, then clamped by D13, rectified by half-wave rectifier D14 and filtered by R90, R91, R77 and C42 to provide a negative DC voltage proportional to the final audio with about an 80ms time constant. This zero to -2V control voltage is applied to the gate of Q22. With no signal present, the DC output is zero, which turns on Q22, forcing R80 to be placed across R70, resulting in a decay time of about 100ms. When a signal is present, the large negative gate to source voltage turns Q22 off, thus removing R80 and extending the time constant of the AGC.

For SSB mode, the AGCSlow control bit is set high, turning off Q3 and removing R77 from the circuit. This increases the time constant to about 500ms.

Preamp AGC equalization

When preamps are engaged, the signal entering the receiver increases. This would normally cause the S-meter to read differently depending on whether you have zero, one or two preamps engaged. Although it is common for radios to show different signal strengths with preamps on and off, it really does not make sense for them to behave this way, because the S-meter is supposed to be an indication of received strength at the antenna input, with a 50uV (-73dBm) signal representing S9 on the meter. To equalize the readings, a DAC output, buffered and inverted through op-amp U4 (GADJ, Sheet 8 of Rx Board) is used to control the drain-source channel resistance of JFET Q19, which in turn controls the gain of amplifier Q6.

A N-channel JFET is turned completely on when the gate-source voltage is zero, and it has a higher resistance as the gate goes negative with respect to the source until it reaches a cutoff threshold which turns it off completely. Thus, different voltages are applied when the preamps are set to off, 1 or 2. A different gain is needed in AM mode. All 4 settings are changeable in a menu option and set during a calibration step.

Muting and de-sense

When operating in Full Break-in mode, in which you want to hear the receiver between dots in CW mode, it is necessary to keep the transmitter from saturating the receiver's amplifiers so that recovery time is fast.

Keeping the transmitter out of the receiver's input amplifiers requires shielding, which is accomplished by separating them into different compartments, and isolating them via solid state Transmit/Receive switching. But that's not really enough. The AGC circuitry must be forced into maximum attenuation mode too. This is done by forcing the RFG DAC to maximum, thus setting the AGC to 7V whenever the PTT line is active. This is done in the firmware. However, the Sienna also has a full duplex mode, in which the Receiver is meant to be left on during

transmission. This is commonly used when operating satellites. Since external transverters are often used for this, the transmit and receive frequencies are different, and there is less chance for transmitter bleed-through into the receiver. Thus, if full duplex is selected, the forced 7V AGC condition is not done.

There's one other thing that must be done during non-full-duplex transmit. The receiver cannot help but pick up a little of the transmitted signal, and we do not usually want to hear that in the speakers. Therefore the audio output must be muted during transmit. This is done by Q34 (Sheet 8). The various audio outputs (from the AM detector, SSB/CW detector and FM detector) are amplified by U4 (pins 1,2,3) and fed into P-channel JFET Q34. R100 provides a load, while C127 makes the AC voltage on the gate follow the source, providing a 0V gate-source voltage that keeps the transistor turned on. As long as the LPTT line is high (meaning the transmitter is off), the drain of Q31 will be low, allowing the AC waveform to keep Q34 on. As soon as LPTT goes low (and we're not in full duplex), Q31 goes high, forcing Q34 to pinch off. The time constant formed by C127 and R102 assures that the drain-source junction pinches off slowly, which eliminates an audible click that occurs when an audio signal is switched off abruptly.

Once the audio signal makes it through Q34, it is fed to the back panel and to the internal PC after being attenuated. The signal is quite strong at this point and must be attenuated so as not to overdrive the sound card. In addition, an output impedance of about 600 ohms is desirable. This is done via R44 and R136. The signal is also passed into two Digitally Controlled Pots (DCPs) (U15), which are programmed via the serial bus discussed earlier. These particular pots are used either to feed the monaural receiver signal to both speakers (normal mode) or to remove it from the left speaker and drive only the right speaker (dual receive mode). In addition, pressing the Mute button sets both pots to 0 to remove the receiver signal from the audio path to the volume controls.

Audio mixer

Sheet 9 on the Receiver board takes audio signals from the Receiver, Sidetone from the Controller, PC Audio from the internal PC or Line-In audio from an external source, and mixes them in audio mixer U11 (pins 1,2,3, 5,6,7). Capacitors C95 and C96 provide one pole of frequency rolloff at about 6KHz. The right channel drives Line-Out to the transmitter (and note that since this can include the Sidetone as well as the receiver, it is possible to transmit code via SSB or AM, and to re-transmit receive audio if full-duplex is enabled).

Volume controls

The outputs of the audio mixer are fed into two more sets of DCPs, one for the speaker volume controls and one for the headphone volume controls. The output of one speaker channel is buffered and level shifted by Q16 to provide an AntiVOX output that is then fed into an A/D converter in the Controller's Keyer microprocessor.
The other half of U11 is used to drive the headphones, and one additional pole of frequency rolloff is provided. The speaker audio is amplified by U18 and U19 to provide 1.5W of stereo with high drive capability. Since the speakers have good audio frequency response up to 20KHz and

there's only one pole on the amplifiers, the audio response has a fair amount of treble. This helps maintain good frequency response when the PC sound card is played through the speakers. However it can cause the receiver to have higher pitch than may be comfortable. The solution is to mute the receiver and use the line out to the internal or external PC sound card, and to run the audio through a DSP such as SiliconPixels' ChromaSound software, which is included when you buy the PC option. Another alternative is to use the graphic equalizer on the sound card to reduce high frequencies.

FM

FM receive is accomplished via an FM receiver chip, the NXP SA615 (Sheet 3). This chip requires a local oscillator and a wideband input signal. To accomplish this, LO3, at 9.455MHz, is split into two paths (Sheet 5). One path drives the mixer that it used for AM/CW/SSB (U5) and it is also fed into pin 4 (FMOSC) of the SA615. The input signal is fed in at 9MHz, which provides a 455KHz difference frequency on the output. This 9MHz signal is derived from the 70.455MHz first IF by routing it through a 70.7MHz low pass filter (to remove sum products from the U6 mixer), and another Gilbert cell mixer, U22, which provides 10dB of gain too. LO3, at 61.455MHz, combines with the 70.455MHz IF to provide a final difference frequency of 9MHz. The output is bandpass filtered by a 500KHz bandwidth filter and fed into the SA615.

The mixer output of the SA615 is a wideband signal at 455KHz. That signal is split into two paths by transformer T2. One leg transforms the impedance from 1800 to 50 ohms via split-C filter C141, C64 and is then fed to a connector on the back panel. The other leg passes though a 20KHz ceramic filter and back into the SA615 for detection. A squelch input is provided by output B of DAC U23 (Sheet 8), whose level is set by the FM squelch control on the front panel. Comparator U29 compares this voltage with that of the RSSI (relative signal strength indicator) output of the SA615 to provide the squelch signal. The detected audio output is fed to the audio amplifier stages by R30 (Sheet 8).

Detectors

Sheet 7 shows the AM, CW and SSB detectors. AM, CW and SSB are present at the XFO1 signal. AM is routed through diodes D16 and D19 when control signal ModeAM is high. The AM signal is then given one last boost by U26 before being detected by the voltage doubler/half-wave rectifier formed by D6 and D15. R22 and C15 filter the high mixing products out, leaving only audio.

CW and SSB signals are routed to the product detector/BFO (U7) after passing one final 20KHz ceramic bandpass filter to clean up any remaining mixing products. U7 is another Gilbert cell mixer with >10dB of gain. LO4 is set to 455KHz (+/-, depending on the pitch and/or sideband that's desired). The resulting output has sum products removed by the pi-network consisting of C153, RFC1 and C6, leaving only audio.

Metering

CMOS switch U21 (Sheet 7) selects either the S-meter or the FM relative signal strength indica-

tor (RSSI) or the output of DAC U23 (TxMeter) to drive one or both analog meters. TxMeter is a calculated value and depends on the meter function that is selected (SWR, Forward Power, PA Volts, etc.).

Transmitter: Transmitter, TxBPF and 100W PA boards

Refer to the block diagram on page xxx and schematics starting on page xxx.

The transmitter in the Sienna is completely separate from the receiver. They do not share local oscillators or bandpass filters as is the case in most transceivers. This allows the transmitter and receiver to be operated at the same time, i.e. in full duplex mode, a useful mode for satellite operations in particular, where you need to be able to listen to your downlinked signal while transmitting. It's also useful if you should want to transmit audio code practice on AM, or retransmit receiver audio on a different frequency.

Microphone and Line Processing

Sheet 1 shows audio input circuitry. The microphone (mic) input is buffered by U9, and resistors R123 and R124 create an input impedance of 100K ohms, suitable for any low-Z microphone and most older high-Z mics like the Astatic D-104. R125 and C81 form a single pole low pass filter with a 3dB breakpoint of 2.3KHz to provide suppression of high frequencies in the audio signal. The output is also fed through a high pass filter to provide "pre-emphasis" for FM and fed to the Controller board via the Receiver board where the signal is used for VOX detection in SSB mode and sampled at an 8KHz rate for FM transmission. The sampled mic data is used to directly change the frequency of the DDS chip that controls the transmitter's VFO. This is true FM, not the Phase Modulation employed by most transmitters. (Frequency is the first derivative of phase, and it is often easier to change the phase of a signal than its frequency, so it is not unusual to condition a PM signal so that it can be received as FM. However the Sienna's DDS chips and audio sampling A/D are fast enough to do true frequency modulation in real time.)

Line/Mic selection

The audio is then fed into a CMOS analog switch (U12, Sheet 2). This switch selects either the mic or the line input from the audio mixer on the Receiver board. This line level input is the audio mix of the PC's line out, the back panel's Line In, the sidetone and the receiver audio. Typically, digital modes will come from either the External Line In or the internal PC's Line out.

Balanced Modulator and CW keying

The selected input is fed into the balanced modulator (U7). Pot RV1 is used in a calibration step to null the carrier in SSB modes. In AM, the balance is removed by turning on Q24, allowing the carrier to feed through. The local oscillator, TXBFO, runs at about 10.7MHz. Thus the first IF is 10.7MHz +/- audio frequencies.

In CW and FM modes, the LO is switched to Q21. The keying circuit (Q19, Q23) waveshapes the keying signal via low pass filter consisting of C9 and R20 and applies it to the drain of Q21. The waveshaped CW signal then appears at the source of Q21. PIN diode D14 keeps the RF from bleeding through to the subsequent stages when the transistor is off.

In FM mode, the key is turned on and TXBFO is frequency modulated based on the amplitude of the sampled microphone input.

SSB/AM filtering

The DSB signal from U7 (107A) is applied to a 7-element variable bandwidth Cohn-style crystal filter. ZC934A varactor diodes are used to change the interstage capacitance and thus change the bandwidth, simply by varying the voltage to the varactors. This design was patented by a Ten-Tec engineer in the early 90's, and is used with Ten-Tec's permission. For SSB use, the LO is shifted above or below the crystal filter's bandwidth to pick off just the desired sideband. For AM use, the filter is bypassed by routing U7's complementary output (107B) through relay K14, where it can be fed into the speech processor and subsequent circuitry.

RF Speech Processor/Buffer/Drive

If the RF speech processor is enabled (Proc control bit) in SSB mode, K11 switches on, and the 107S signal is passed through the speech processor circuit before being routed to buffer amp Q15. The SSB signal is amplified by U17, an NXP SA603 voltage-controlled amplifier. The processor level control on the front panel causes output "D" of DAC U5 (Sheet 6) to be changed from 2.5V to 3.5V as the control is moved from 0 to full scale. This changes the gain of this amplifier by up to 50dB, resulting in a strong signal that is clipped by Schottky diodes D1 and D2. Transformer T2 samples the compression and boosts it by a factor of 6, where diode D23 rectifies it and R80 and C131 filter it to produce a DC voltage that is directly proportional to the level of RF compression. That signal, CMPR, is fed into a buffer op-amp (U4, Sheet 9), where it is protected against overvoltage and fed to an A/D converter on the Controller board. The clipped signal is buffered by Q15 (Sheet 4) and then fed into a seven element fixed crystal filter, which removes the high order mixing products caused by the clipping. This results in an RF compression of up to 15dB. The output is fed to the drive control via a Darlington transistor, Q27, which allows the high crystal filter impedance to be matched while providing low impedance drive for the RF mixer.

IF CW or FM are in use, the waveshaped signal CWRF is fed through a 20kHz ceramic filter to remove harmonic content, and then through Darlington transistor buffer Q30. Q27 and Q30 cannot both be on at the same time, as controlled by AMSSB and CWFM control voltages. The resulting output of CW, FM, AM, or SSB appears at AMFO and drives another variable gain amplifier, which we call the Drive, providing a strong signal, MTX, for TUF-3 mixer U10.

VFO, Bandpass filters

The VFO is fed into U10 (Sheet 5) along with the selected SSB, CW, AM or FM (carrier) signal. The difference product is bandpass filtered by the TXBPF board located at J13. This board is identical to the ones used on the RXBPF board for the receiver discussed earlier. The only difference is that the TXBPF board selects the band based on 4 bits of band data from U1 (Sheet 8). This band data is compatible with that used by Yaesu's linear amplifiers.

Voltage Controlled Amplifier, ALC

The bandpass filtered signal from J13 is next fed into another NXP SA603 voltage controlled amplifier (U8). The BUFALC control voltage (Sheet 9) provides the 2.5V to 3.5V required to change the gain of this amplifier over a 10dB range (well less than its maximum 30dB range).

K13 (Sheet 9) selects either the internal 0-4.1V ALC control voltage from output A of DAC U5 (Sheet 6) or an external ALC voltage from an external amplifier. The 0 to –4.1V voltage provided by most amplifiers is inverted first by U11 (Pins 5,6,7). The selected ALC voltage is then passed through differential amplifier U11 (pins 1,2,3) where it is divided by 4.1 and then subtracted from a DAC voltage PWRSET, nominally 3.5V, resulting in the 2.5V to 3.5V control voltage for U8. This amplifier (U8) along with the drive amplifier, are the sole sources of transmitter power gain.

Transverter output

The 1mW output of U8 is amplified by Q14 by about 10dB and then transformer coupled to the power amps. It is also buffered by Darlington transistor Q31 to provide a transverter output.

Driver

Sheet 6 shows the power amplifier stages. Q3 amplifies the signal up to 1 Watt, which is then coupled into the paralleled final amplifiers consisting of Q4 and Q5. Q3's bias point is changed from Class B (for CW and FM modes) to Class AB for SSB and AM modes. This is done by U6 and Q8, with DAC output D serving only as an extra control bit to turn Q8 on and off. When the transmitter is off (output of Q16, PTT, low), Q38 is off, so U6 (pins 1,2,3) is at a low voltage that is insufficient to bias Q3, keeping any low level RF from feeding through. When Q38 turns on, the bias voltage from the finals is multiplied by 5.7 and applied to Q3's bias resistors R10 and R11.

10Watt PA

The 1W output of the driver is fed into Q4 and Q5, which are out of phase with each other by 180 degrees thanks to toroid transformer T3. The outputs are recombined by T5 to produce the final 10 Watt output signal. Transformer T4 serves as the DC collector inductor for both transistors. A portion of the output signal is sampled by one-turn windings on the secondary of T5 and fed back to the inputs to provide some automatic level control. Back to back zener diodes on the secondary of T3 keep the input voltage in a safe range to protect final transistors Q4 and Q5, which have 5V max ratings on their base-emitter junctions.

The DC bias point for the final transistors is provided by pass transistor Q6 and regulating transistor Q12. The TXPVCC voltage is enabled only when PTT is engaged, via Q13 on Sheet 9. As with the Driver stage, the bias point is set to either Class B or Class AB via R52 and R30.

T/R switch and low pass filters

The 10W output from T5 is fed into one of five low pass filters shown on Sheet 7. If the 100W amplifier is not installed, the bandpass filters are also tapped at the 10W signal point and fed through a transmit/receive PIN diode switch network consisting of diodes D3 and D7, chokes RFC1 and RFC2, and output coupling capacitors C80 and C113. Resistors R40 and R42 bias the PIN diodes at half the supply voltage when enabled by Q1. The low pass filtered receive signal is then passed to the RXBPF board's "Main Antenna" input. Of course, if the rig is used in full duplex mode, this path cannot be used and the receive antenna input is automatically selected to avoid feeding high power RF into the receiver.

The low pass filters are 7-element Elliptical LC filters.

Control logic is shown on Sheet 8 and consists of 8-bit registers that produce the control bits already discussed.

100W amplifier

If the 100W amplifier is installed, the T/R switching is done on this board instead of the transmitter, so the RF cable going to the BPF board is removed from the transmitter (J8) and reconnected to the 100W amp (J6). Similarly, the transmitter output is re-routed from J5 on the DCD/Tuner board to the 10W RF input (J5) on the 100W amp, and the antenna output of the 100W amp (J2) is routed to the DCD/Tuner board's antenna jack (J4).

Fan control

Sheet 1 shows decoding logic, fan control and the high power supply switching. A voltage divider consisting of thermistor TH1, which touches the heatsink, and R28 produces a nominal (cool heatsink) voltage of about 1.09V. The reference input to the comparator is set to 2.88V. As the heatsink gets hot, the thermistor's resistance goes down, increasing the voltage. Capacitor C69 stabilizes the voltage. Once the voltage rises to 2.88V, the comparator's output turns off (open), and current then flows through R31 and the base-emitter junction of Q10, turning on Q10. This shorts out R32 and causes maximum current to flow through the two fans. Resistors R29 and R30 provide hysteresis, which keeps the comparator from oscillating at the trip point. When the fans and/or lack of transmitting reduces the temperature enough, the comparator trips the other direction and restores the fans to idle (low speed).

T/R switching

Unregulated voltage at W1/W2 provides the high current to the final amplifier transistors, and this voltage is not switched. It is present at all times. The amplifier's T/R switch is switched via signal TXPVCC, which is switched by Q3 when the LPTT signal goes low.

Amp bypass

Sheet 2 is the heart of the 100W amplifier. A 10 Watt input signal can either be fed to the amplifier or it can be switched directly to the T/R switch via relays K1 and K2. If the amp is bypassed, the BON signal (derived from the PAON bit before the relay driver on Sheet 1) will stay low, assuring that the amplifier is biased off by U3/Q7. When the amp is enabled, PAON goes high, switching the 10W input signal to the 100W amp and making BON go high, which enables the bias circuit and sets the amplifier for Class B operation. This provides more efficiency that a Class AB amplifier, allowing for higher power out. Class C is usually used in CW modes, but the conservatively rated parts can easily operate in Class B while still providing over 100W out.

Drive reduction at higher frequencies

R17, R18 and C9 form an equalization network to reduce the drive requirement on higher bands.T1 couples the signal into the amplifier.

Final current measurement

U3, R19, R20, Q5 and R21 form a current measurement circuit. When current flows through sense resistor R19, a small voltage is developed across it. Since it is a .005 ohm resistor, a 20A current would result in a 100mV drop. This is small enough not to impact the voltage delivered to the final transistors. The higher voltage side of R19 also appears at R20. Op-amp U3 sees the lower voltage on pin 2, and since an input at the negative terminal also appears at the positive terminal while also providing a high impedance load, the net effect is to mirror the voltage of the sense resistor across R20. Using the previous example, 100mV across the 100 ohm R20 causes 1mA to flow through it. Since the op-amp's + input is also high impedance, that same current must flow through Q5, developing a voltage across R21. (There's also base-emitter current flowing through R21, but it is equal to the collector current divided by the beta of the transistor, and thus can be ignored). 1mA through the 3.16K R21 is 3.16V. Thus, a 20A current flowing to the final transistors is converted to 3.16V for measurement by the microprocessor. The output of Q5 is fed into a series resistor and 5.1V Zener diode to keep the voltage going to the microprocessor from spiking above the microprocessor's rating.

The amplifier

The amplifier transistors are operated in push-pull. A positive swing on the AC input signal on the secondary of T1 is amplified by Q8 but not by Q9. When the AC waveform goes negative, the situation is reversed and Q9 amplifies while Q8 is off. The two halves of the signal are reassembled by transformer T2. The center tap of T2, which is at AC ground by virtue of C6 and C25, feeds the DC supply to the collectors. T2 has a 4:1 turns ratio, so the approximately 24Vp-p maximum swing on the primary appears as 96Vp-p on the secondary. Since transformers do not affect power transfer appreciably (except for some minor losses), the 100Wrms signal that is developed by the primary (24Vp-p = 8.5Vrms; 8.5V*20A = 170W input power; the efficiency is about 60%, which results in about 100Wrms) is also seen at the secondary. With a secondary voltage of 96Vp-p (34Vrms), and with a power level of 100W, the AC current flowing

in the secondary is thus about 3 Amps rms.

Stability filter and T/R switch

RF appearing at K3 is routed to a high pass filter consisting of toroids L14 and L15 and capacitor C70. with a breakpoint at about 1.5MHz. Thus the amplifier cannot be used at full power below this frequency. If the PTT signal is active, the TXPVCC voltage is enabled, and current flows through R23, RFC5, D3, RFC6 and R24, biasing D3 at about 6V and allowing the AC waveform to pass through it via PIN diode action. D3 is large to be able to handle the high AC current.

Low pass filters

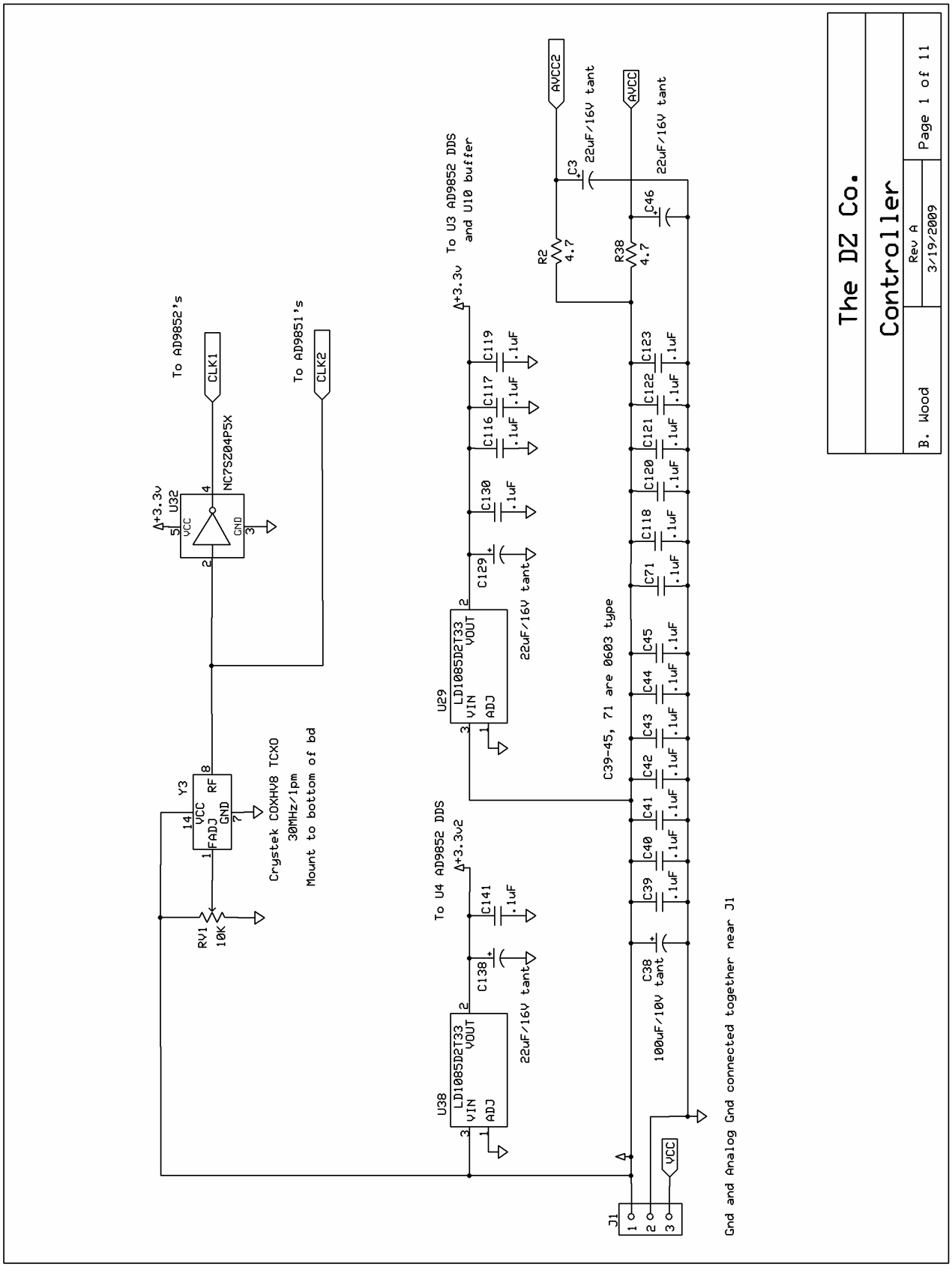
The Xcv output signal is then routed to the low pass filters consisting of L1-L12, K4-K13, and the silver mica capacitors. Control signals from U1 and U2 select one bank of these filters depending on band. The output of the filters is fed to the antenna output.

Receive switching

When the amplifier is not transmitting, the signal appearing at the antenna input is routed through the low-pass filters to the receiver (C21, D5, D13 and C22 on Sheet 4). Since this path must be disabled during transmit, and since high voltage appears at the Xcv point, a circuit consisting of U4 and surrounding parts creates a low current, 100V backbias voltage that keeps D5 and D13 turned off. When PTT is removed, Q1 turns off the backbias circuit and Q2 quickly shunts the voltage to ground, which also allows the normal diode biasing to work, turning on PIN diodes D5 and D13 and passing the signal to the receiver. In order to enable high speed QSK, this solid state T/R switching occurs within 1ms of removal of the PTT signal.

Insert block diagram page here

Schematics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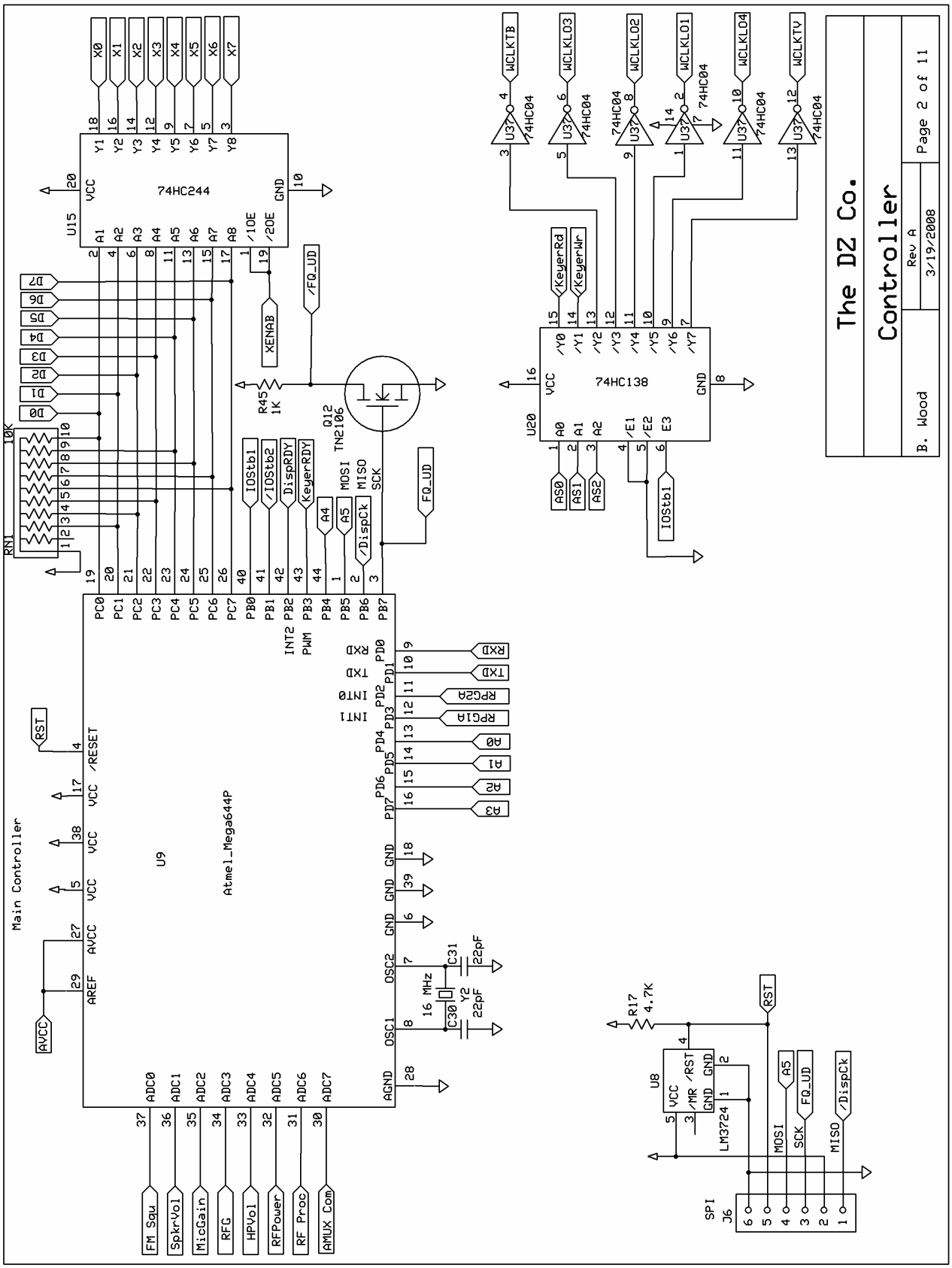
To AD9852's
To AD9851's
CLK1
CLK2
NC7SZ04P5X
U32
+3.3v
VCC
GND
Y3
VCC
ADJ
RF
GND
Crystek COXHV8 TCXO
30MHz/1pm
Mount to bottom of bd
RV1
10K
To U3 AD9852 DDS
and U10 buffer
U29
LD1085D2T33
VIN
VOUT
ADJ
C129
22uF/16V tant
C130
C116
C117
C119
C118
C120
C121
C122
C123
C71
C45
C44
C43
C42
C41
C40
C39
.1uF
C39-45, 71 are 0603 type
AVCC2
AVCC
C3
C46
22uF/16V tant
R2
R38
4.7
To U4 AD9852 DDS
+3.3v2
U38
C141
C138
C38
100uF/10V tant
J1
VCC
Gnd and Analog Gnd connected together near J1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Main Controller
Atmel_Mega644P
U9
74HC244
U15
74HC138
U20
74HC04
U37
LM3724
U8
RN1
10K
R45
1K
R17
4.7K
Q12
TN2106
Y2
16 MHz
C30
C31
22pF
XENAB
/FQ_UD
FQ_UD
IOStb1
/IOStb2
DispRDY
KeyerRDY
/DispCk
MOSI
MISO
SCK
/KeyerRd
/KeyerWr
WCLKTB
WCLKLO3
WCLKLO2
WCLKLO1
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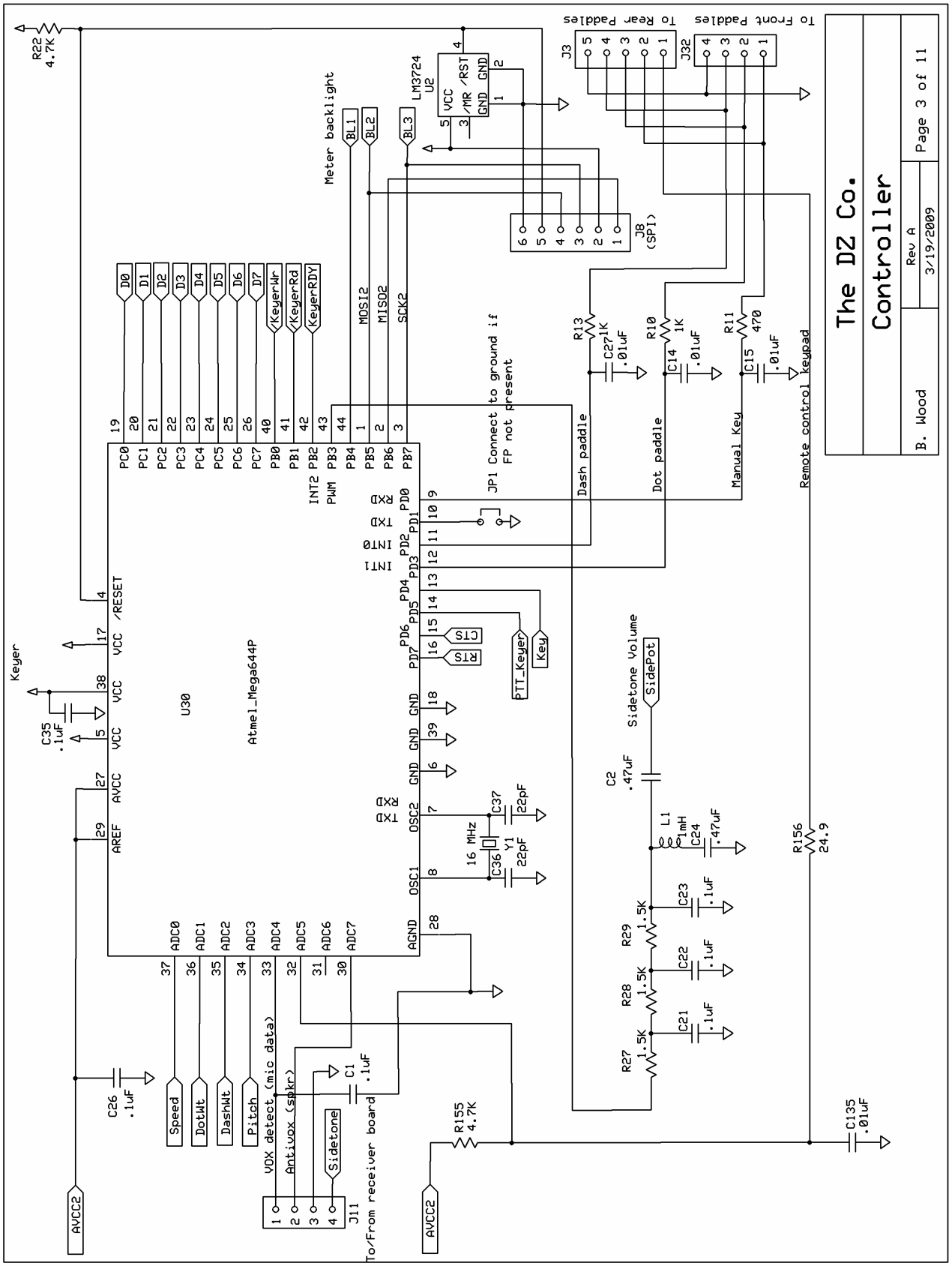
J6
FM Squ
SpkrVol
MicGain
RFG
HPVol
RFPower
RF Proc
AMUX Com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Atmel_Mega644P
U30
Keyer
Meter backlight
To Rear Paddles
To Front Paddles
JP1 Connect to ground if FP not present
Dash paddle
Dot paddle
Manual Key
Remote control keypad
Sidetone Volume
SidePot
PTT_Keyer
Key
CTS
RTS
TXD
RXD
INT0
INT1
INT2
PWM
MOSI2
MISO2
SCK2
KeyerWr
KeyerRd
KeyerRDY
VOX detect (mic data)
Antivox (spkr)
Sidetone
To/From receiver board
Speed
DotWt
DashWt
Pitch
16 MHz
LM3724
J8 (SPI)
J3
J32
J11
R22 4.7K
R155 4.7K
R156 24.9
R27 1.5K
R28 1.5K
R29 1.5K
R13 1K
R10 1K
R11 470
C35 .1uF
C26 .1uF
C1 .1uF
C21 .1uF
C22 .1uF
C23 .1uF
C24 .47uF
C2 .47uF
C27 .01uF
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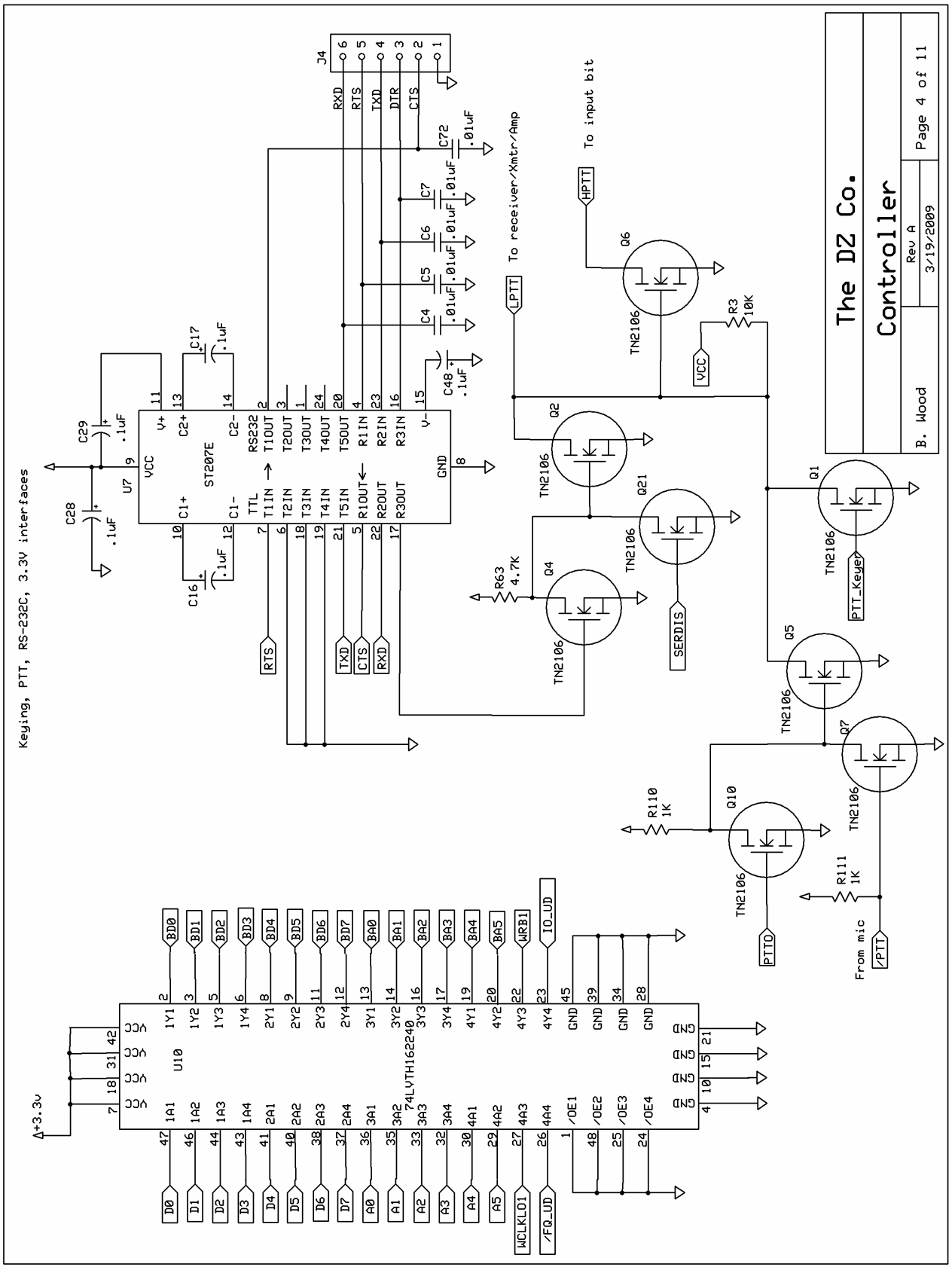
C36 22pF
C37 22pF
Y1
L1 1mH
AVCC2


Keying, PTT, RS-232C, 3.3V interfaces
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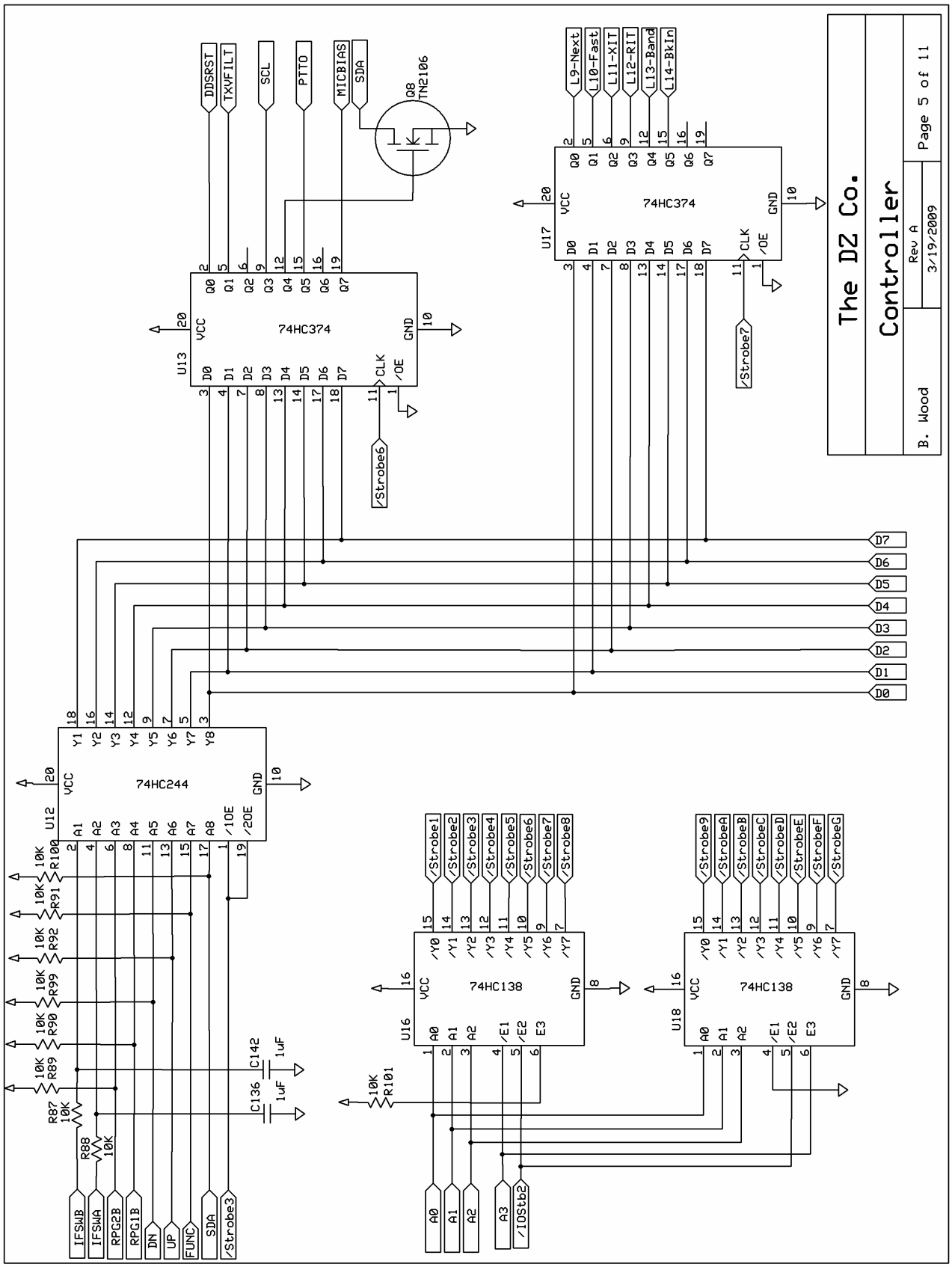
ST207E
74LVTH16240
TN2106
To receiver/Xmtr/Amp
To input bit
From mic
SERDIS
PTT_Keyer
WCLKLO1
/FQ_UD
IO_UD
+3.3v
VCC
GND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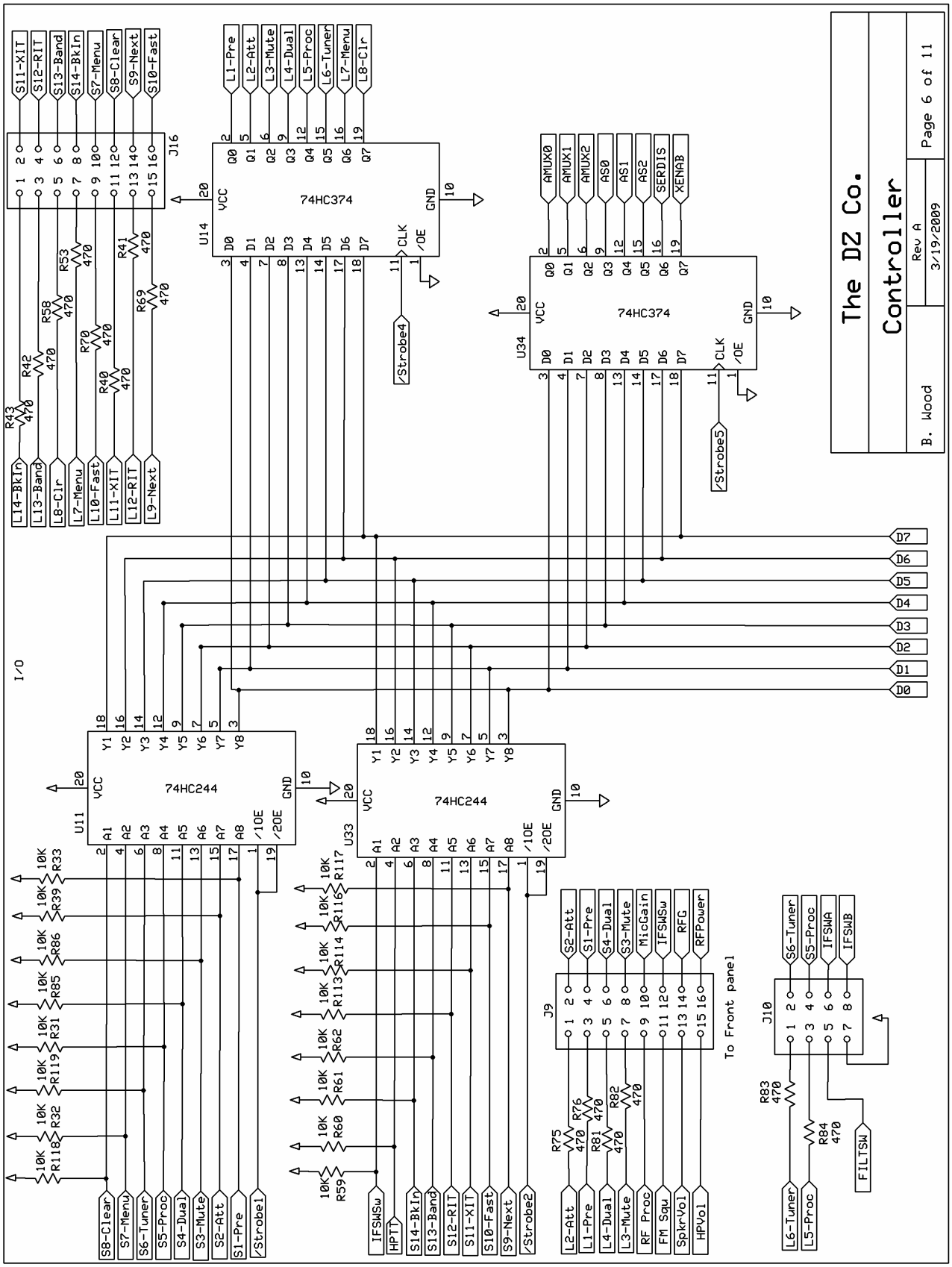
74HC374
74HC244
74HC138
DDSRST
TXVFILT
SCL
PTTO
MICBIAS
SDA
Q8
TN2106
L9-Next
L10-Fast
L11-XIT
L12-RIT
L13-Band
L14-BkIn
/Strobe6
/Strobe7
D0
D1
D2
D3
D4
D5
D6
D7
IFSWB
IFSWA
RPG2B
RPG1B
DN
UP
FUNC
SDA
/Strobe3
A0
A1
A2
A3
/IOStb2
C142
1uF
C136
1uF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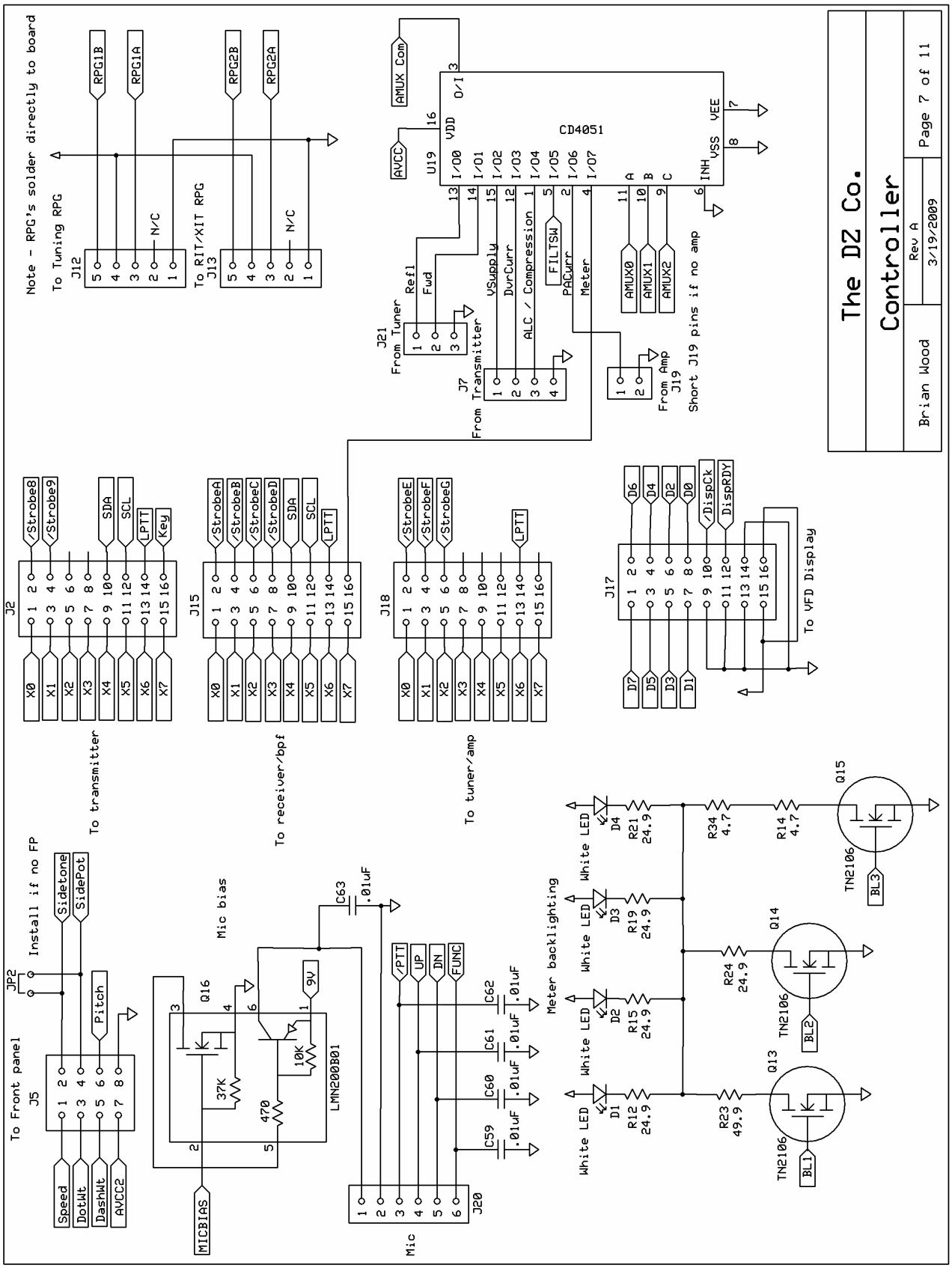
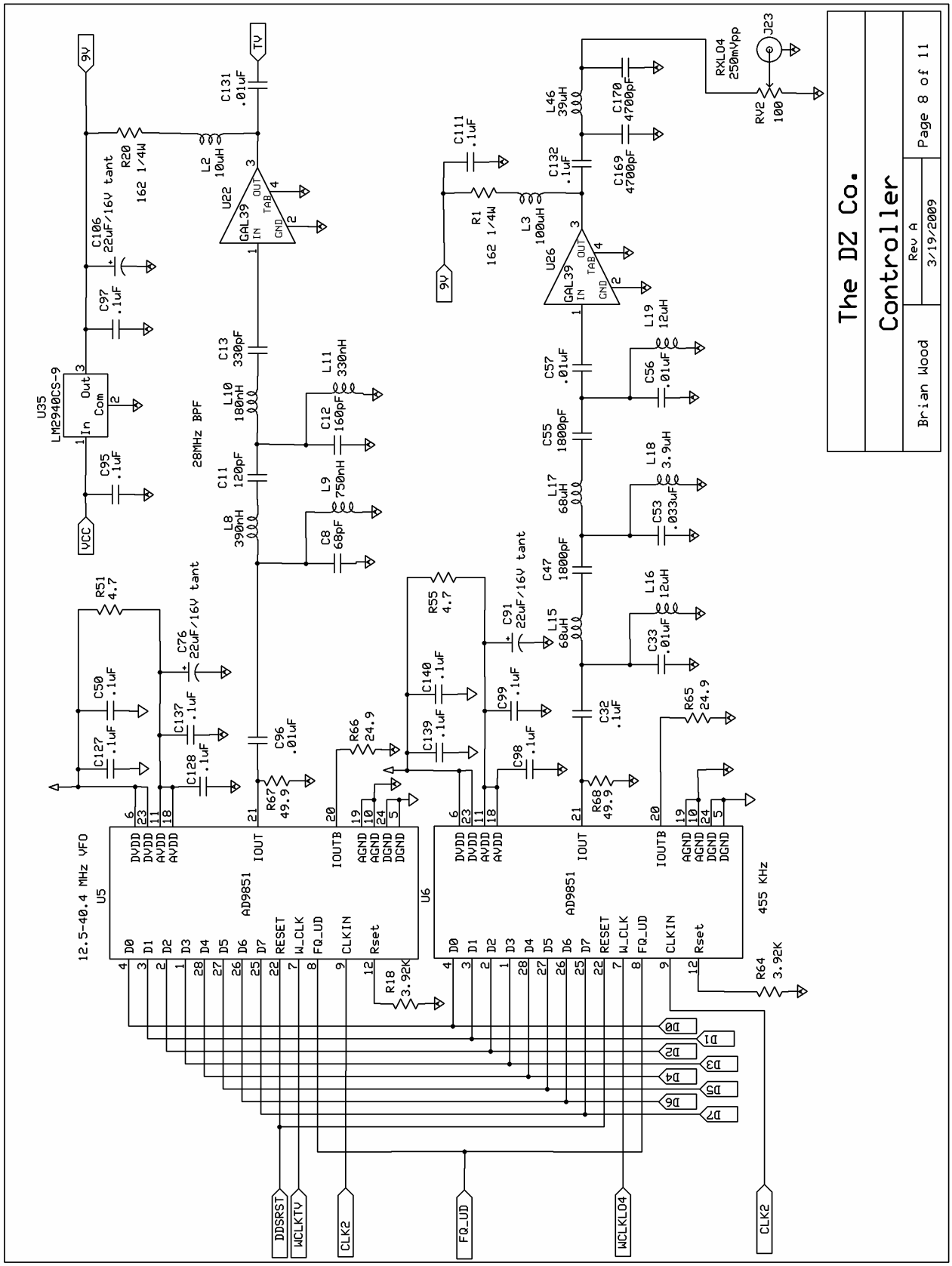
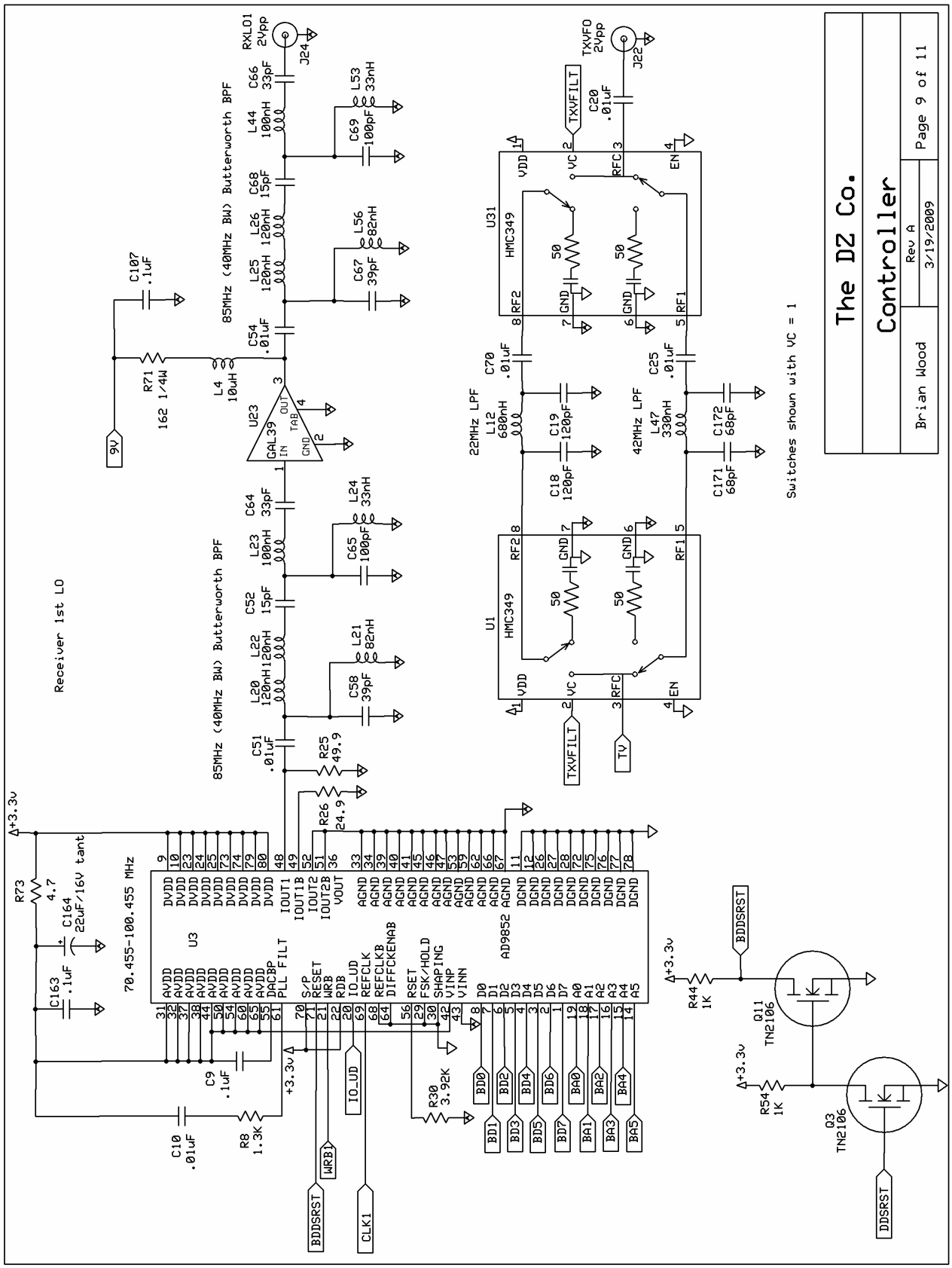
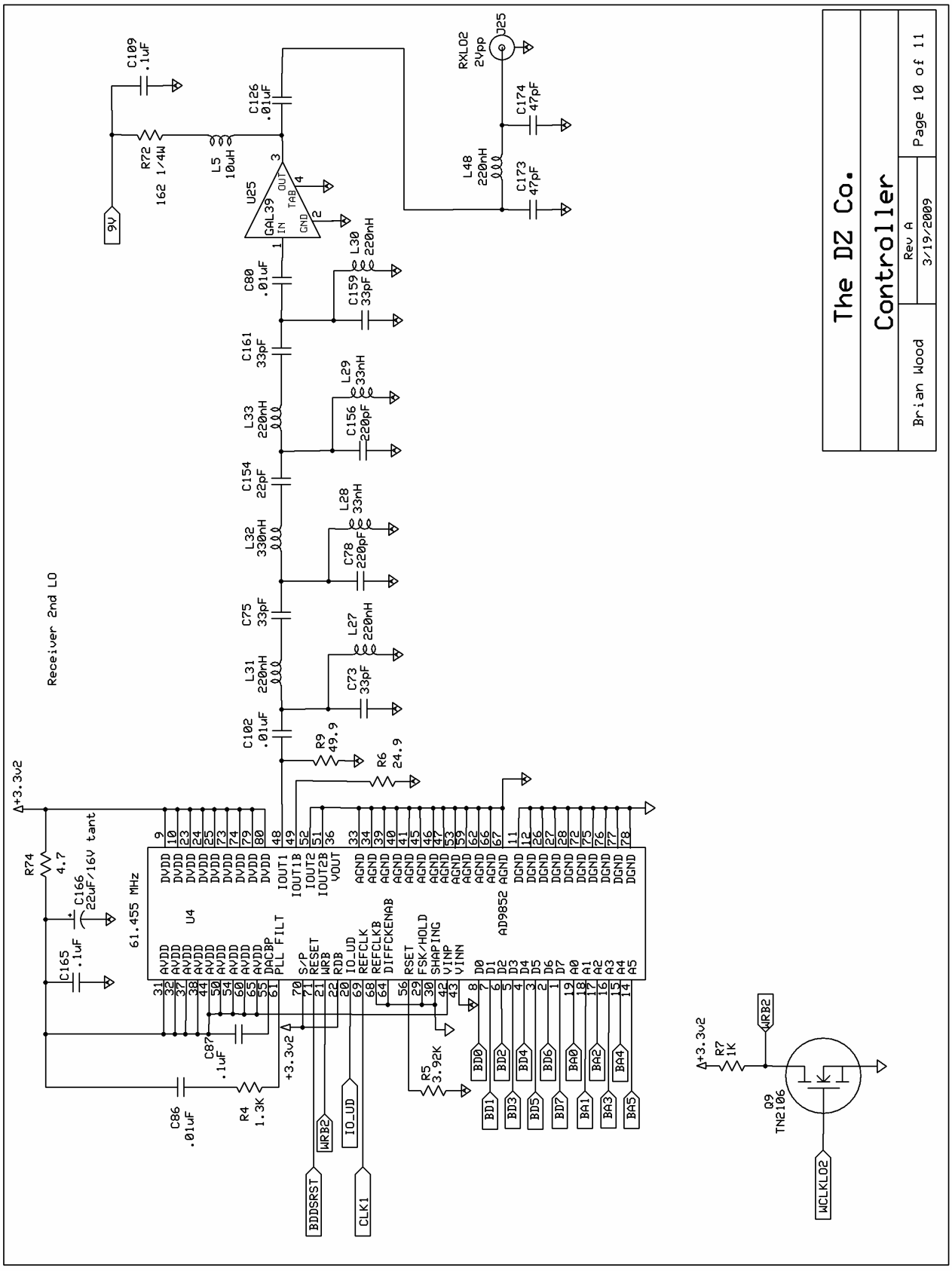
74HC374
74HC244
I/O
To Front panel


The DZ Co.
Controller
Brian Wood
Rev A
3/19/2009
Page 7 of 11
Note - RPG's solder directly to board
To Tuning RPG
J12
To RIT/XIT RPG
J13
RPG1B
RPG1A
RPG2B
RPG2A
N/C
CD4051
AMUX Com
AVCC
VDD
VEE
VSS
INH
From Tuner
J21
From Transmitter
J7
From Amp
J19
Short J19 pins if no amp
FILTSW
AMUX0
AMUX1
AMUX2
To transmitter
To receiver/bpf
To tuner/amp
To VFD Display
To Front panel
J5
Install if no FP
JP2
Sidetone
SidePot
Pitch
Speed
DotWt
DashWt
AVCC2
Mic bias
MICBIAS
Mic
J20
LMN200B01
Meter backlighting
White LED
TN2106
Q13
Q14
Q15
Q16


The DZ Co.
Controller
Brian Wood
Rev A
3/19/2009
Page 8 of 11
12.5-40.4 MHz VFO
455 KHz
28MHz BPF
AD9851
U5
U6
U22
U26
U35
GAL39
LM2940CS-9
9V
5V
VCC
RXLO4
250mVpp
J23
RV2
100
R1
162 1/4W
R20
162 1/4W
L2
10uH
L3
100uH
L46
39uH
C131
.01uF
C111
.1uF
C106
22uF/16V tant
C97
.1uF
C95
.1uF
C132
.1uF
C169
4700pF
C170
4700pF
C13
330pF
C12
160pF
C11
120pF
C8
68pF
L10
180nH
L11
330nH
L9
750nH
L8
390nH
C57
.01uF
C56
.01uF
C55
1800pF
C53
.033uF
L19
12uH
L18
3.9uH
L17
68uH
C47
1800pF
L16
12uH
L15
68uH
C33
.01uF
C32
.1uF
C91
22uF/16V tant
C76
22uF/16V tant
C50
.1uF
C127
.1uF
C137
.1uF
C128
.1uF
C96
.01uF
C140
.1uF
C139
.1uF
C99
.1uF
C98
.1uF
R51
4.7
R55
4.7
R66
24.9
R67
49.9
R68
49.9
R65
24.9
R18
3.92K
R64
3.92K
DVDD
AVDD
IOUT
IOUTB
AGND
DGND
D0
D1
D2
D3
D4
D5
D6
D7
RESET
W_CLK
FQ_UD
CLKIN
Rset
DDSRST
WCLKTV
CLK2
FQ_UD
WCLKLO4
CLK2


The DZ Co.
Controller
Brian Wood
Rev A
3/19/2009
Page 9 of 11
Receiver 1st LO
70.455-100.455 MHz
85MHz (40MHz BW) Butterworth BPF
85MHz (40MHz BW) Butterworth BPF
22MHz LPF
42MHz LPF
Switches shown with VC = 1
U1
U3
U23
U31
AD9852
HMC349
GAL39
RXLO1 2Vpp
TXVFO 2Vpp
TXVFILT
TV
9V
+3.3v
BDDSRST
DDSRST
WRB1
CLK1
IO_UD
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BA0
BA1
BA2
BA3
BA4
BA5
Q3 TN2106
Q11 TN2106


The DZ Co.
Controller
Brian Wood
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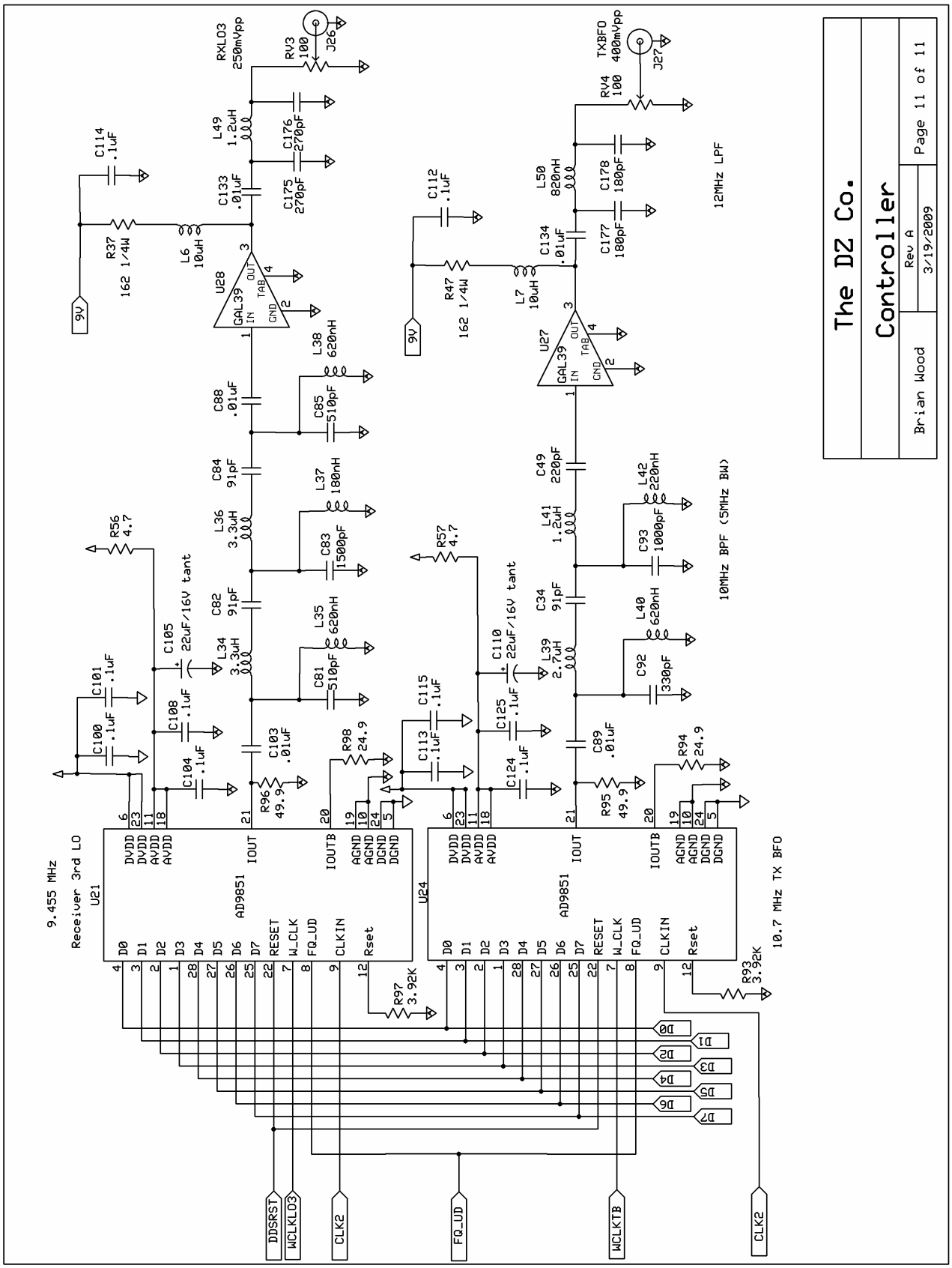
Page 10 of 11
Receiver 2nd LO
61.455 MHz
AD9852
U4
U25
GAL39
9V
RXLO2
2Vpp
J25
+3.3v2
WRB2
IO_UD
BDDSRST
CLK1
WCLKLO2
Q9
TN2106


The DZ Co.
Controller
Brian Wood
Rev A
3/19/2009
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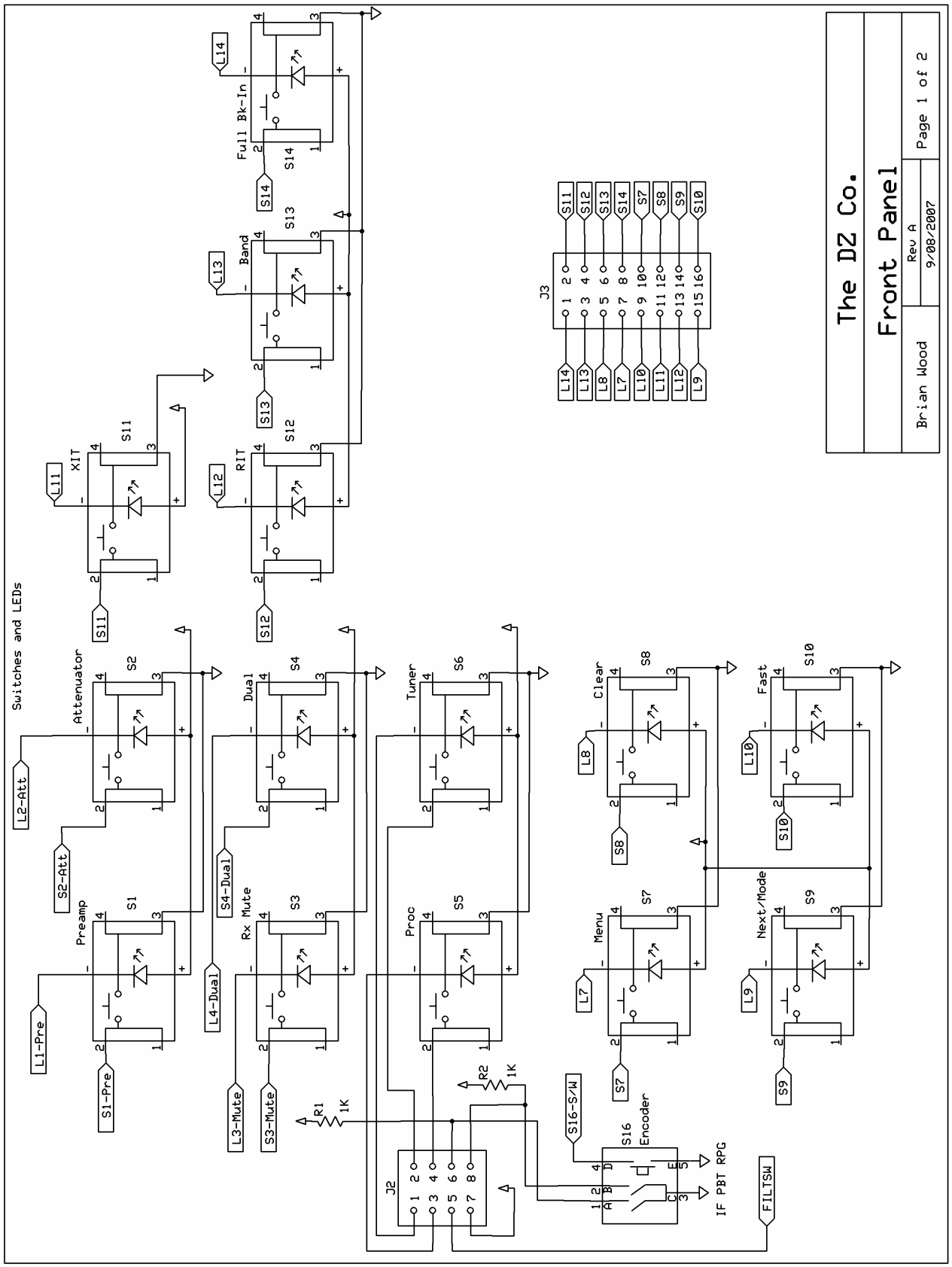
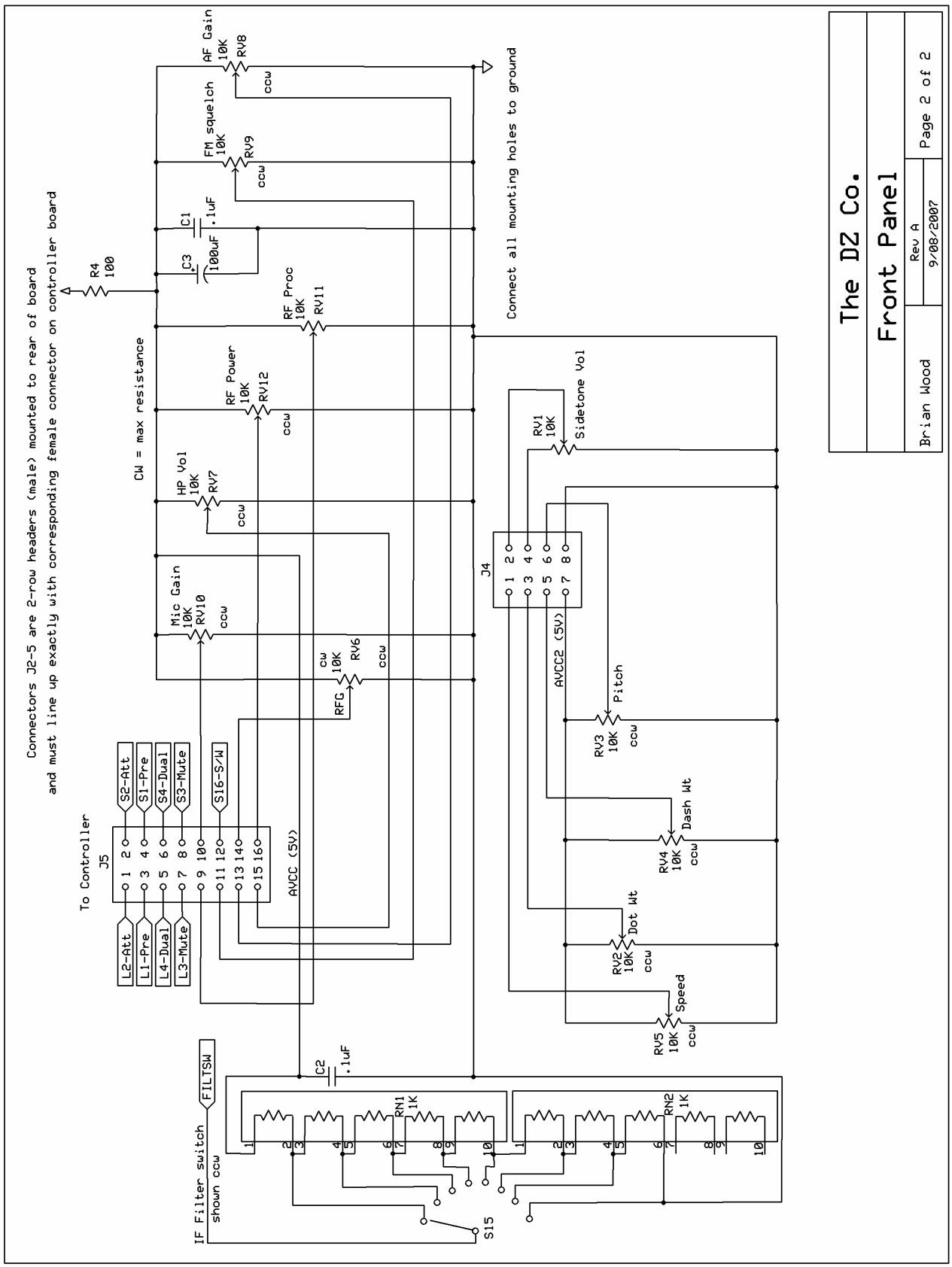
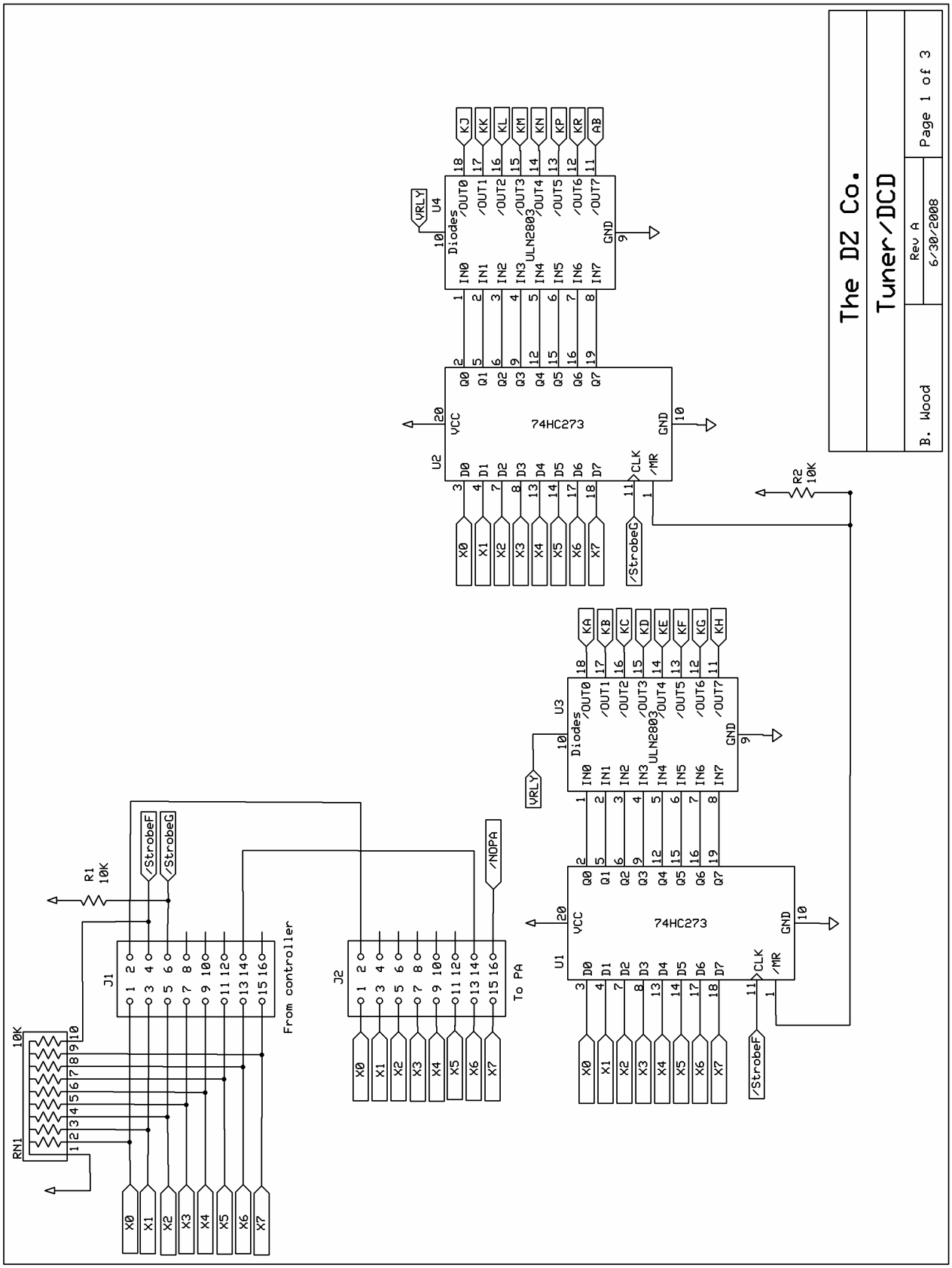
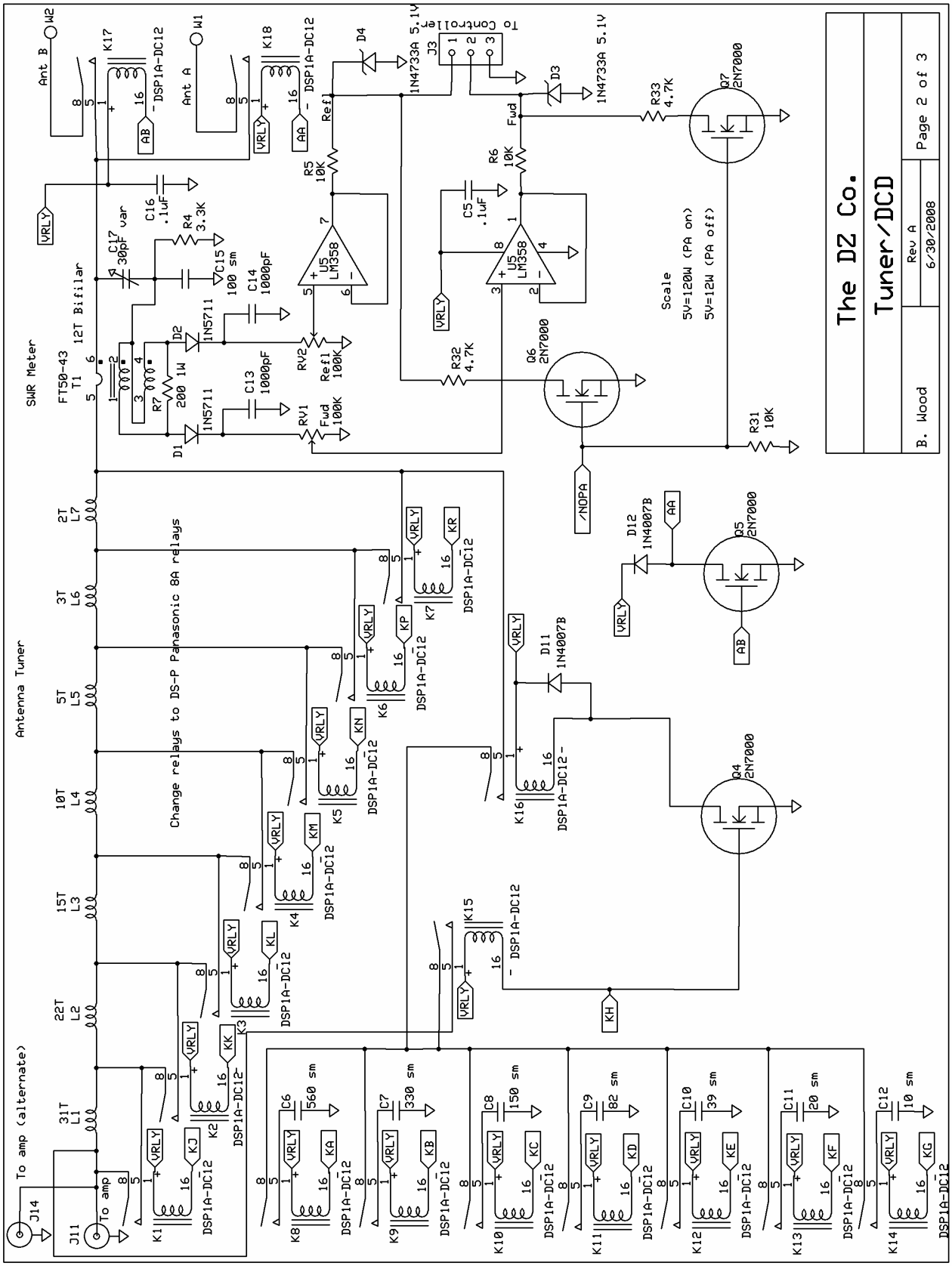
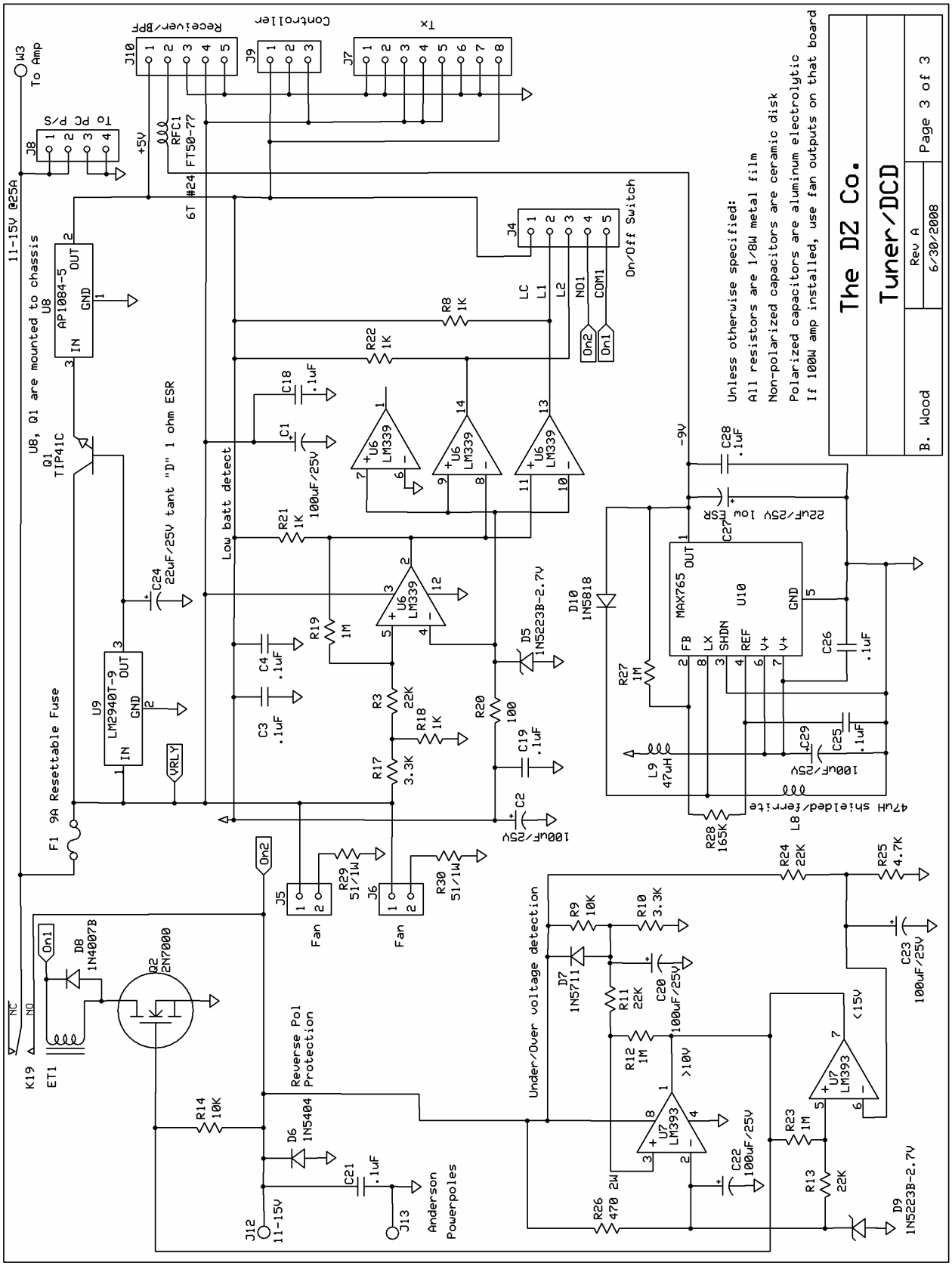
9.455 MHz
Receiver 3rd LO
10.7 MHz TX BFO
10MHz BPF (5MHz BW)
12MHz LPF
RXLO3
250mVpp
TXBFO
400mVpp
AD9851
U21
U24
U28
U27
GAL39
DDSRST
WCLKLO3
CLK2
FQ_UD
WCLKTB

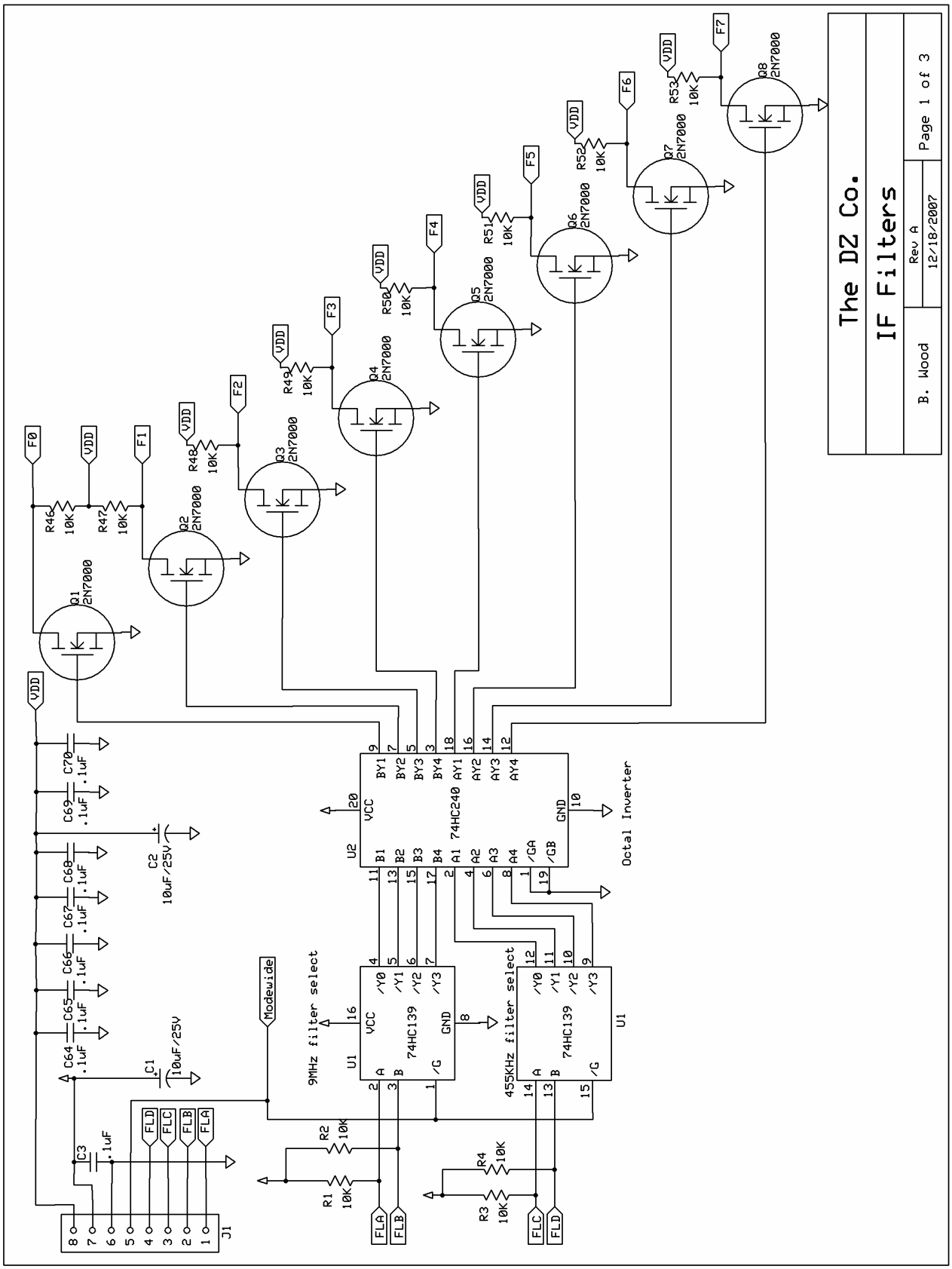

The DZ Co.
Front Panel
Brian Wood
Rev A
9/08/2007
Page 1 of 2
Switches and LEDs
Attenuator
Preamp
Dual
Rx Mute
Tuner
Proc
Clear
Menu
Fast
Next/Mode
Band
Full Bk-In
XIT
RIT
S16 Encoder
S16-S/W
IF PBT RPG
FILTSW
R1 1K
R2 1K
J2
J3

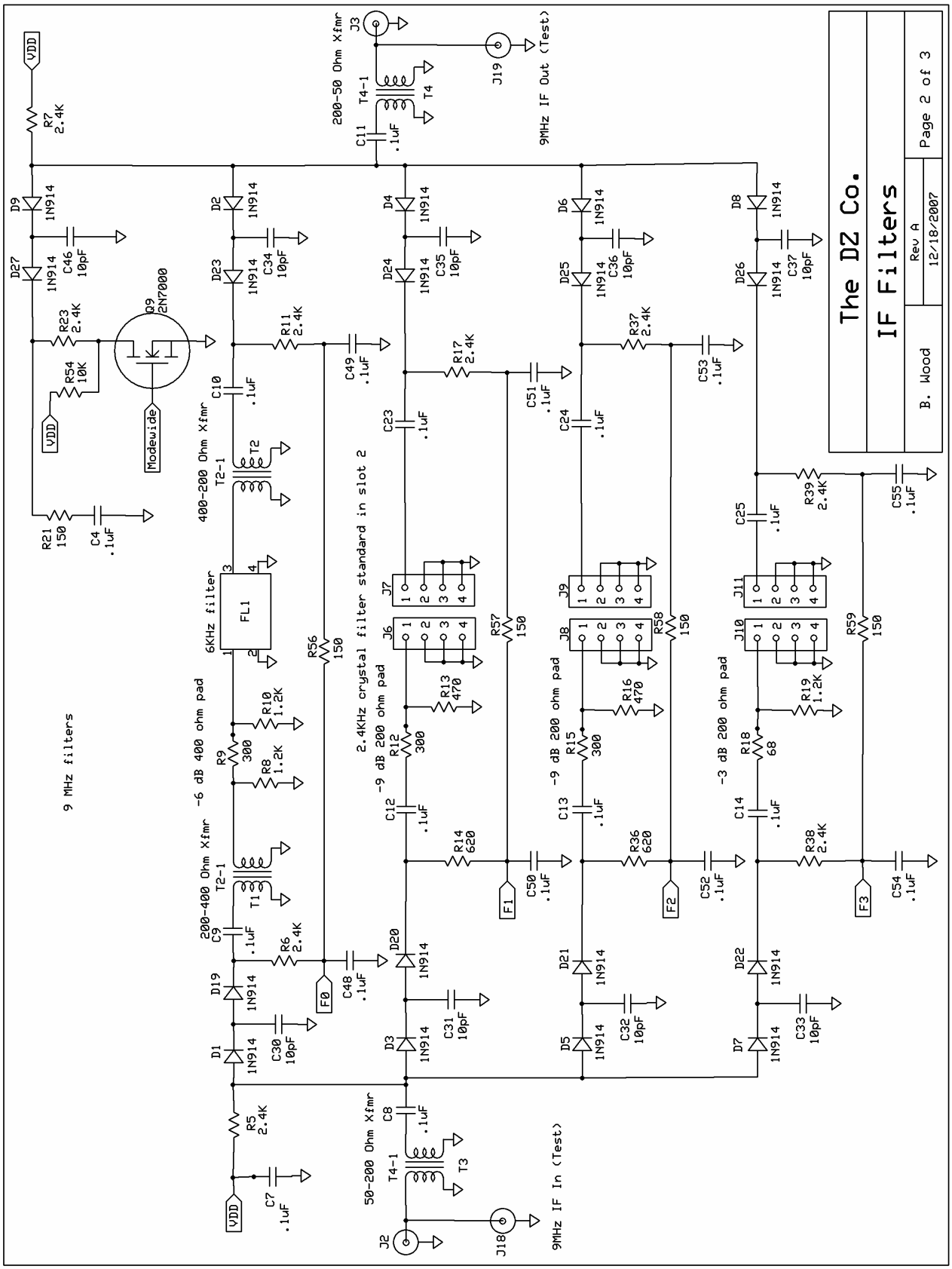

The DZ Co.
Front Panel
Brian Wood
Rev A
9/08/2007
Page 2 of 2
Connectors J2-5 are 2-row headers (male) mounted to rear of board
and must line up exactly with corresponding female connector on controller board
CW = max resistance
Connect all mounting holes to ground
To Controller
J5
J4
AF Gain 10K RV8 ccw
FM squelch 10K RV9 ccw
C1 .1uF
C3 100uF
R4 100
RF Proc 10K RV11
RF Power 10K RV12 ccw
HP Vol 10K RV7 ccw
Mic Gain 10K RV10 ccw
RV1 10K Sidetone Vol
RFG cw 10K RV6 ccw
AVCC (5V)
AVCC2 (5V)
RV3 10K Pitch ccw
RV4 10K Dash Wt ccw
RV2 10K Dot Wt ccw
RV5 10K Speed ccw
S2-Att
S1-Pre
S4-Dual
S3-Mute
S16-S/W
L2-Att
L1-Pre
L4-Dual
L3-Mute
C2 .1uF
RN1 1K
RN2 1K
FILTSW
IF Filter switch shown ccw
S15


The DZ Co.
Tuner/DCD
B. Wood
Rev A
6/30/2008
Page 1 of 3
74HC273
ULN2803
Diodes
VRLY
/StrobeF
/StrobeG
/StrobeG
/NOPA
R1
10K
R2
10K
RN1
10K
J1
J2
From controller
To PA
U1
U2
U3
U4
VCC
GND
CLK
/MR
/OUT0
/OUT1
/OUT2
/OUT3
/OUT4
/OUT5
/OUT6
/OUT7
IN0
IN1
IN2
IN3
IN4
IN5
IN6
IN7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
D0
D1
D2
D3
D4
D5
D6
D7
X0
X1
X2
X3
X4
X5
X6
X7
KA
KB
KC
KD
KE
KF
KG
KH
KJ
KK
KL
KM
KN
KP
KR
AB


The DZ Co.
Tuner/DCD
B. Wood
Rev A
6/30/2008
Page 2 of 3
Antenna Tuner
SWR Meter
Change relays to DS-P Panasonic 8A relays
To amp (alternate)
To amp
Ant A
Ant B
To Controller
Scale
5V=120W (PA on)
5V=12W (PA off)
FT50-43
T1
12T Bifilar
31T L1
22T L2
15T L3
10T L4
5T L5
3T L6
2T L7
Ref1
Fwd
VRLY
/NOPA
1N4733A 5.1V
DSP1A-DC12
LM358
2N7000
1N4007B
1N5711


The DZ Co.
Tuner/DCD
Rev A
6/30/2008
B. Wood
Page 3 of 3
Unless otherwise specified:
All resistors are 1/8W metal film
Non-polarized capacitors are ceramic disk
Polarized capacitors are aluminum electrolytic
If 100W amp installed, use fan outputs on that board
11-15V @25A
W3 To Amp
J8 P/S PC TO
J10 Receiver/BPF
J9 Controller
J7 Tx
+5V
RFC1 FT50-77
6T #24
J4 On/Off Switch
LC L1 L2 NO1 COM1
On2 On1
U8 AP1084-5 IN OUT GND
U8, Q1 are mounted to chassis
Q1 TIP41C
U9 LM2940T-9 IN OUT GND
F1 9A Resettable Fuse
VRLY
C24 22uF/25V tant "D" 1 ohm ESR
Low batt detect
C1 100uF/25V
C18 .1uF
R8 1K
R22 1K
R21 1K
U6 LM339
C4 .1uF
C3 .1uF
R19 1M
R3 22K
R18 1K
R17 3.3K
R20 100
C19 .1uF
C2 100uF/25V
D5 1N5223B-2.7V
-9V
C28 .1uF
C27 22uF/25V low ESR
D10 1N5818
U10 MAX765 FB LX SHDN REF V+ V+ GND OUT
C26 .1uF
R27 1M
L9 47uH
C29 C25 .1uF 100uF/25V
L8 47uH shielded/ferrite
R28 165K
R24 22K
R25 4.7K
C23 100uF/25V
J5 J6 Fan Fan
R29 51/1W
R30 51/1W
On2
On1
D8 1N4007B
Q2 2N7000
NC NO
K19 ET1
Reverse Pol Protection
R14 10K
D6 1N5404
C21 .1uF
J12 11-15V
J13 Anderson Powerpoles
Under/Over voltage detection
R9 10K
R10 3.3K
D7 1N5711
C20 100uF/25V
R11 22K
R12 1M
>10V
U7 LM393
C22 100uF/25V
R26 470 2W
<15V
R23 1M
R13 22K
D9 1N5223B-2.7V


The DZ Co.
IF Filters
B. Wood
Rev A
12/18/2007
Page 1 of 3
Octal Inverter
9MHz filter select
455KHz filter select
Modewide
74HC240
74HC139
2N7000
VDD
GND
VCC


The DZ Co.
IF Filters
B. Wood
Rev A
12/18/2007
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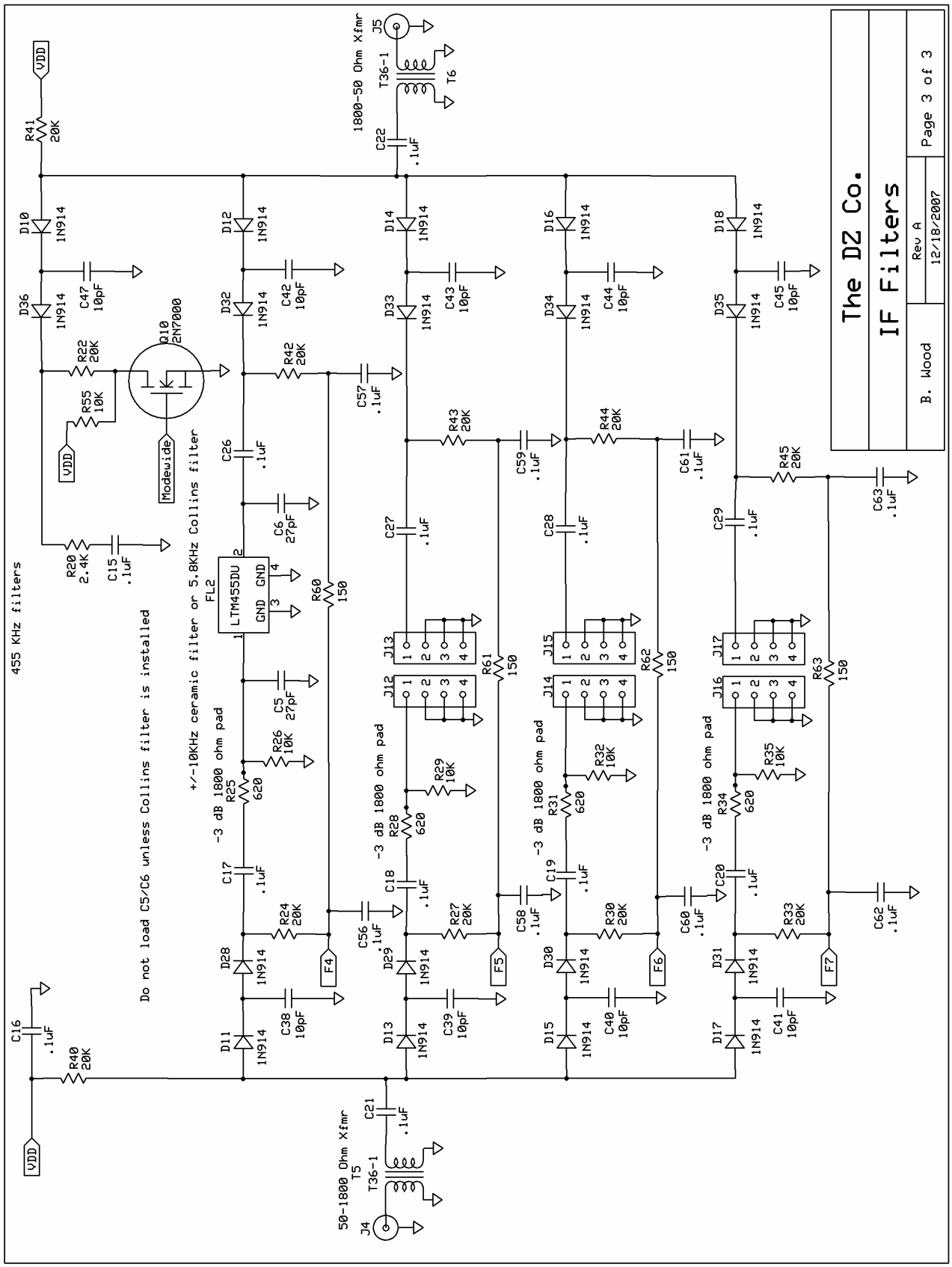
9 MHz filters
9MHz IF Out (Test)
9MHz IF In (Test)
200-50 Ohm Xfmr
50-200 Ohm Xfmr
200-400 Ohm Xfmr
400-200 Ohm Xfmr
6KHz filter
2.4KHz crystal filter standard in slot 2
-6 dB 400 ohm pad
-9 dB 200 ohm pad
-9 dB 200 ohm pad
-3 dB 200 ohm pad
Modewide
VDD


The DZ Co.
IF Filters
B. Wood
Rev A
12/18/2007
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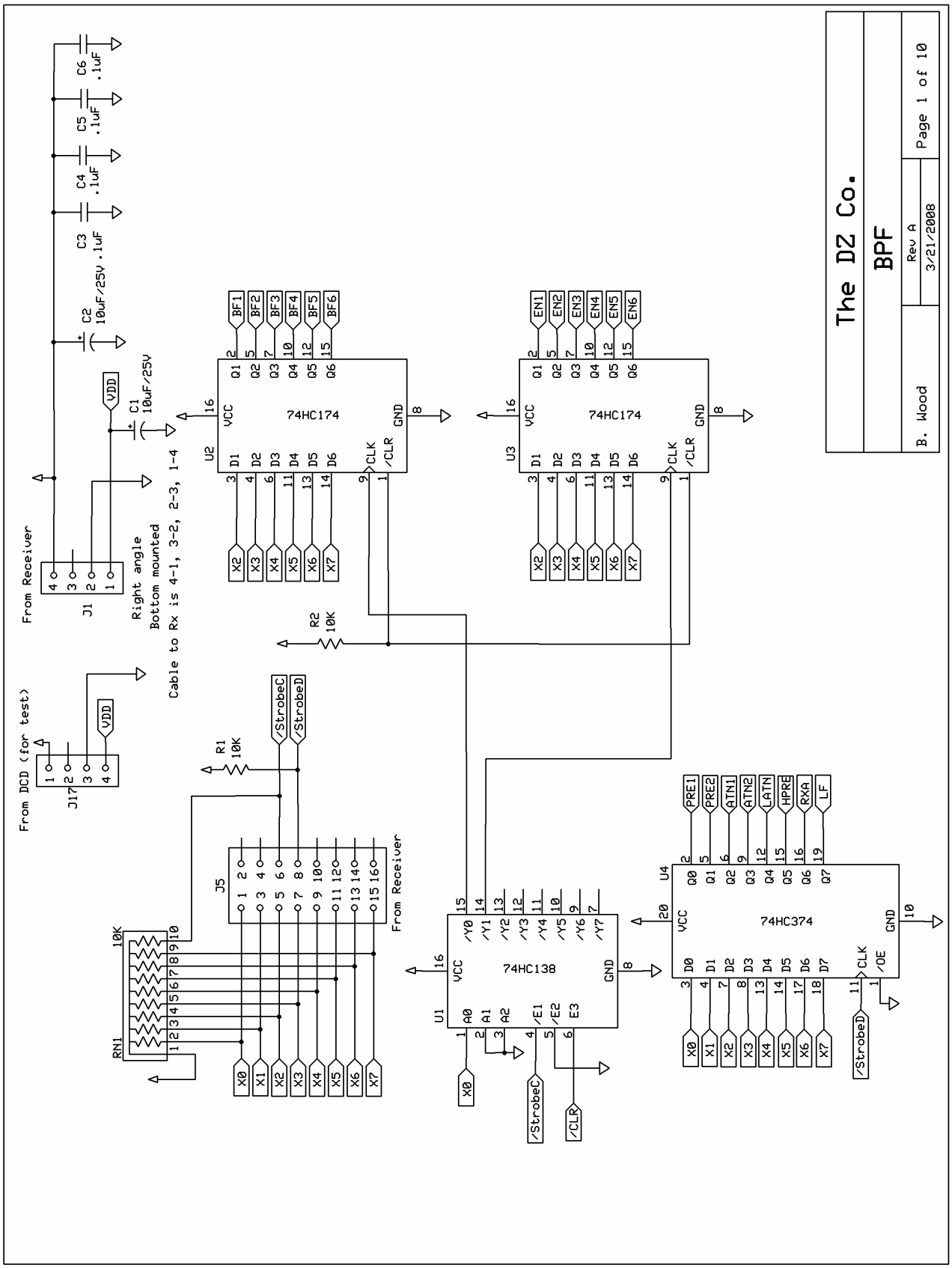
455 KHz filters
Do not load C5/C6 unless Collins filter is installed
+/-10KHz ceramic filter or 5.8KHz Collins filter
FL2
LTM455DU
-3 dB 1800 ohm pad
1800-50 Ohm Xfmr
50-1800 Ohm Xfmr
Modewide
VDD
Q10
2N7000
F4
F5
F6
F7


The DZ Co.
BPF
Rev A
3/21/2008
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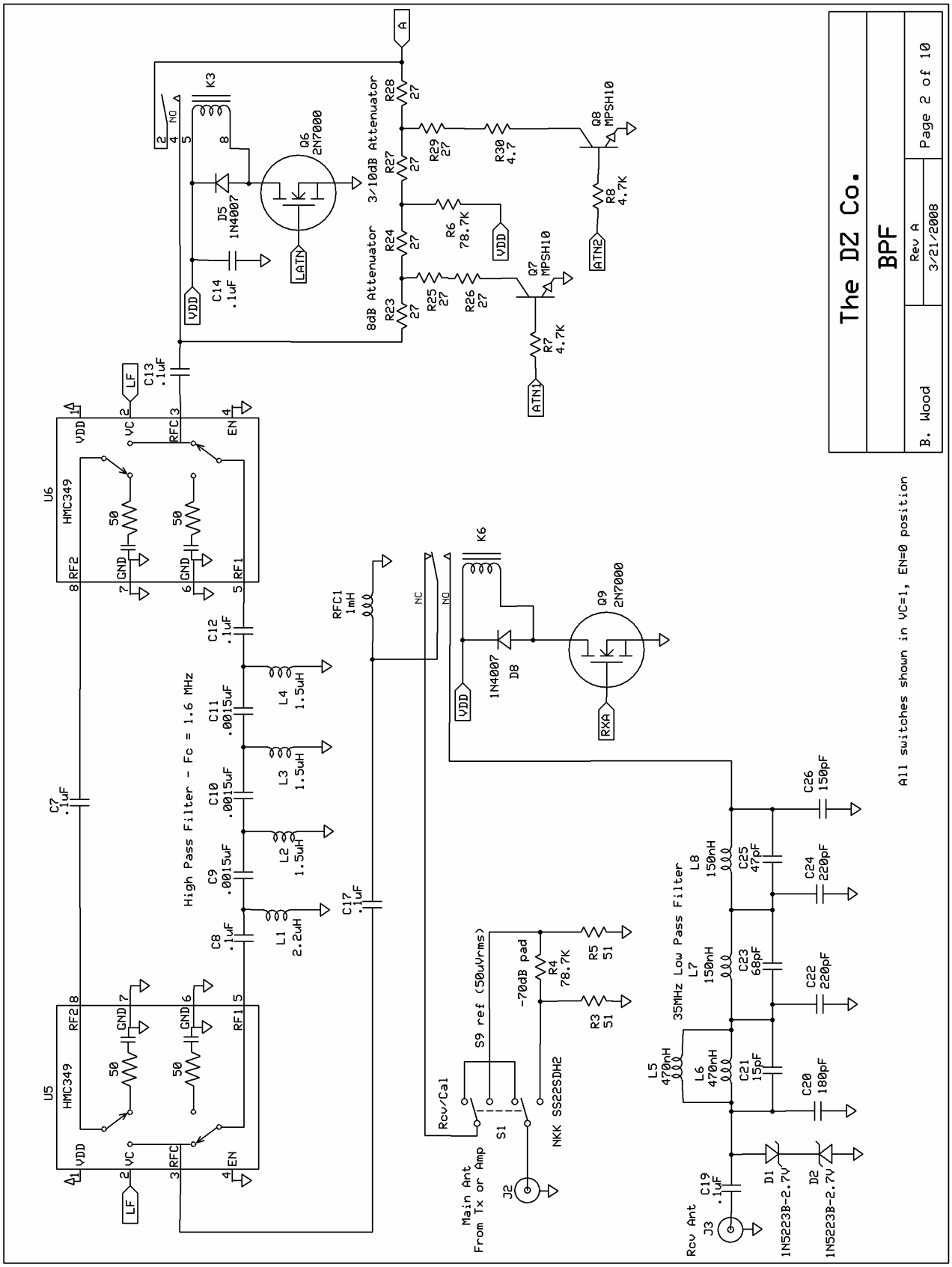
B. Wood
74HC174
74HC138
74HC374
From Receiver
Right angle
Bottom mounted
Cable to Rx is 4-1, 3-2, 2-3, 1-4
From DCD (for test)
From Receiver
VDD
/StrobeC
/StrobeD
/CLR


The DZ Co.
BPF
Rev A
3/21/2008
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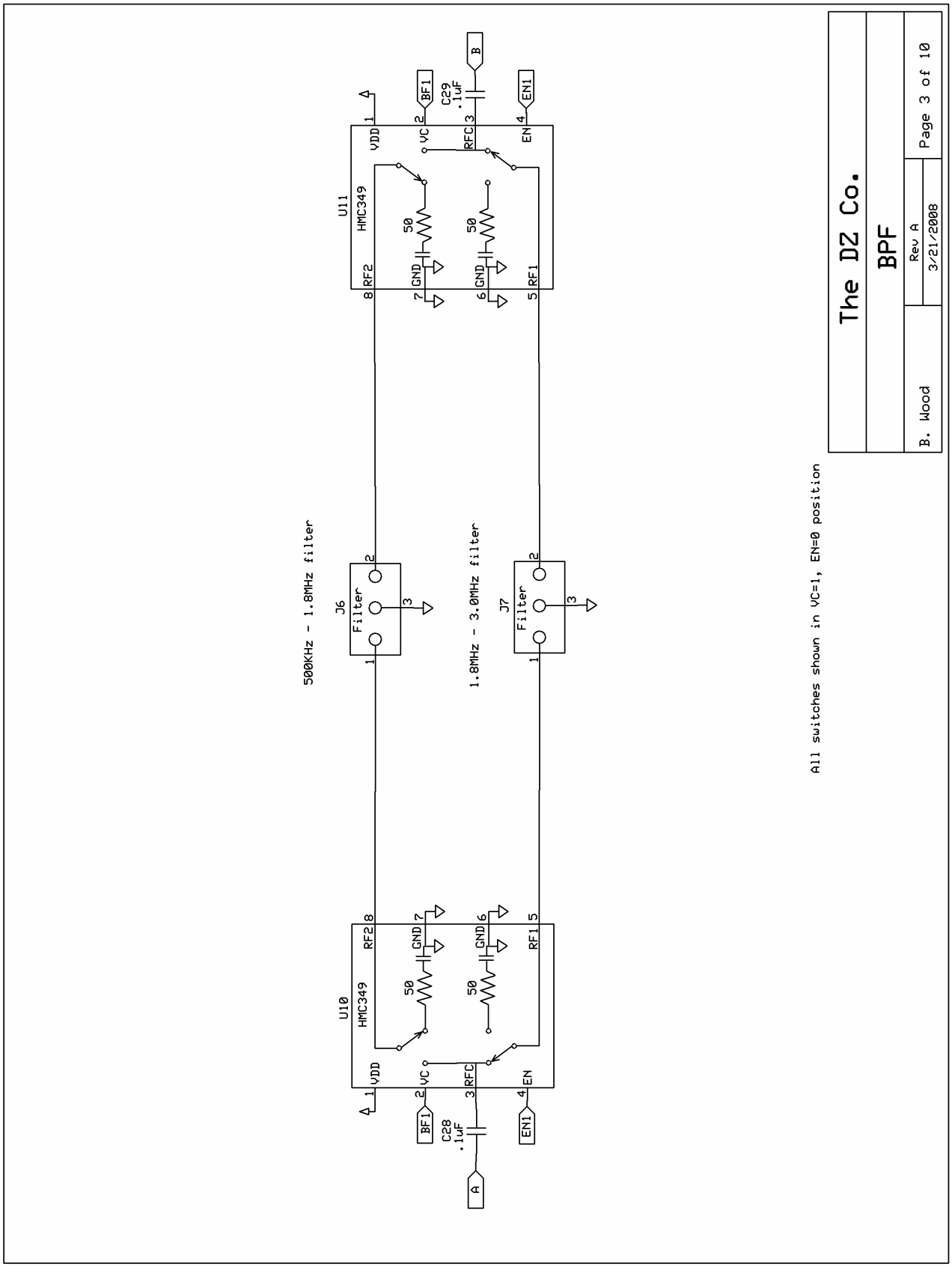
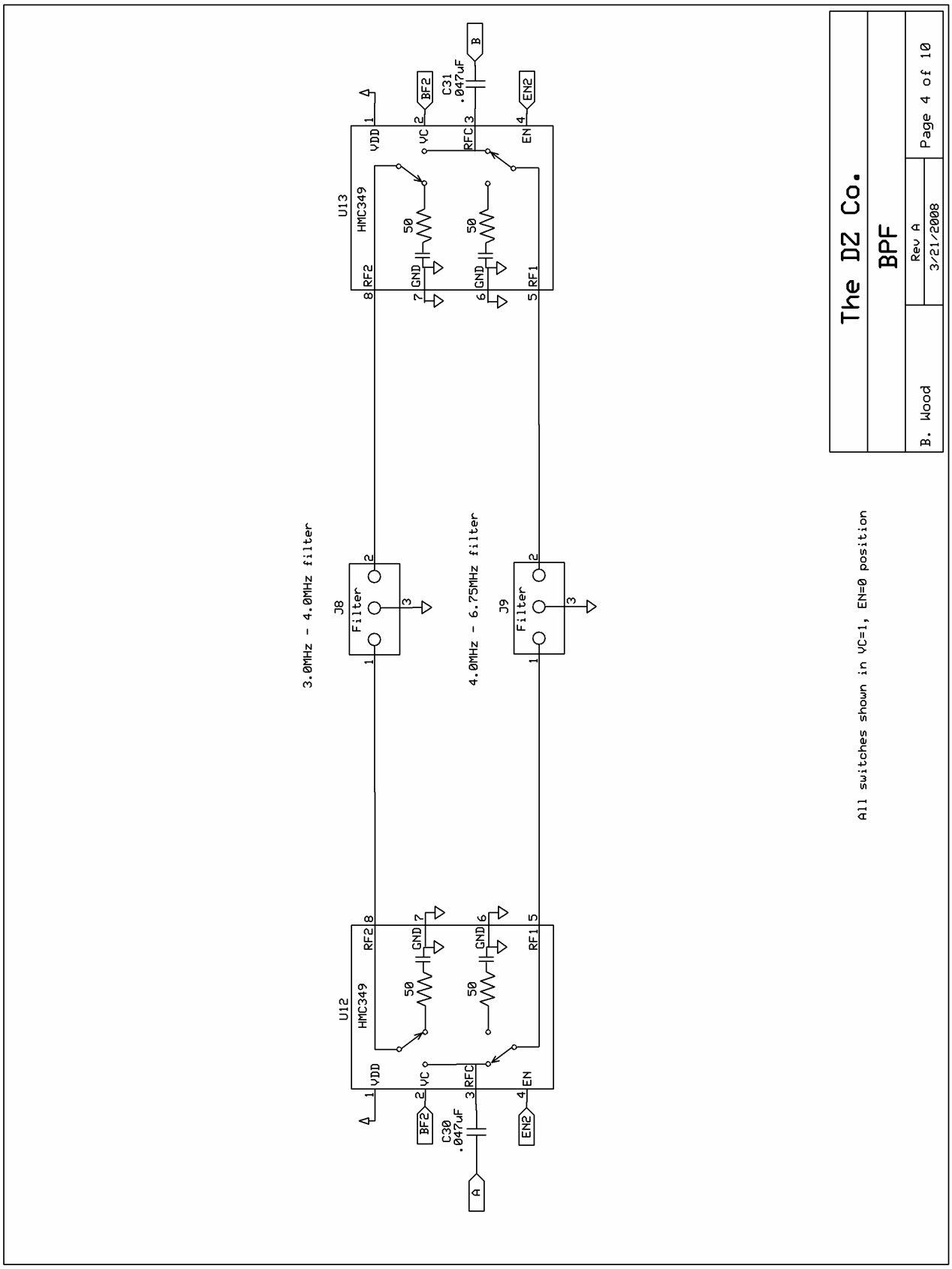
B. Wood
All switches shown in VC=1, EN=0 position
High Pass Filter - Fc = 1.6 MHz
35MHz Low Pass Filter
8dB Attenuator
3/10dB Attenuator
-70dB pad
S9 ref (50uVrms)
Rcv/Cal
Main Ant
From Tx or Amp
Rcv Ant
NKK SS22SDH2
HMC349
1N4007
2N7000
MPSH10
1N5223B-2.7V
VDD
LF
VC
RFC
EN
RF1
RF2
GND
LATN
ATN1
ATN2
RXA


The DZ Co.
BPF
B. Wood
Rev A
3/21/2008
Page 3 of 10
All switches shown in VC=1, EN=0 position
500KHz - 1.8MHz filter
1.8MHz - 3.0MHz filter
U10
U11
HMC349
VDD
VC
RFC
EN
RF1
RF2
GND
50
J6
J7
Filter
A
B
BF1
EN1
C28
C29
.1uF


The DZ Co.
BPF
Rev A
3/21/2008
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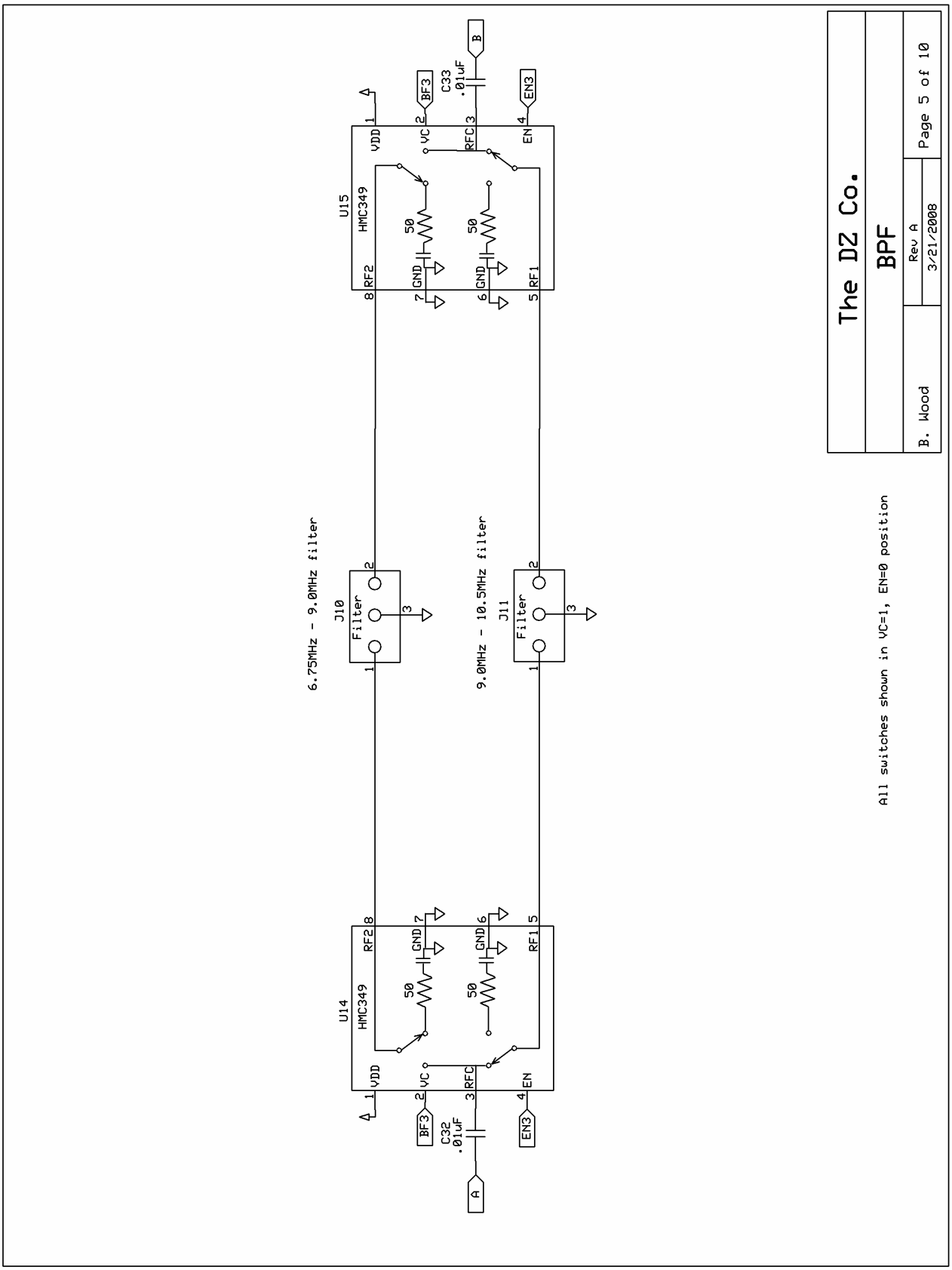
B. Wood
All switches shown in VC=1, EN=0 position
3.0MHz - 4.0MHz filter
4.0MHz - 6.75MHz filter
U12
HMC349
U13
HMC349
J8
J9
Filter
VDD
RF2
RF1
RFC
VC
EN
GND
50
BF2
EN2
A
B
C30
.047uF
C31
.047uF


The DZ Co.
BPF
Rev A
3/21/2008
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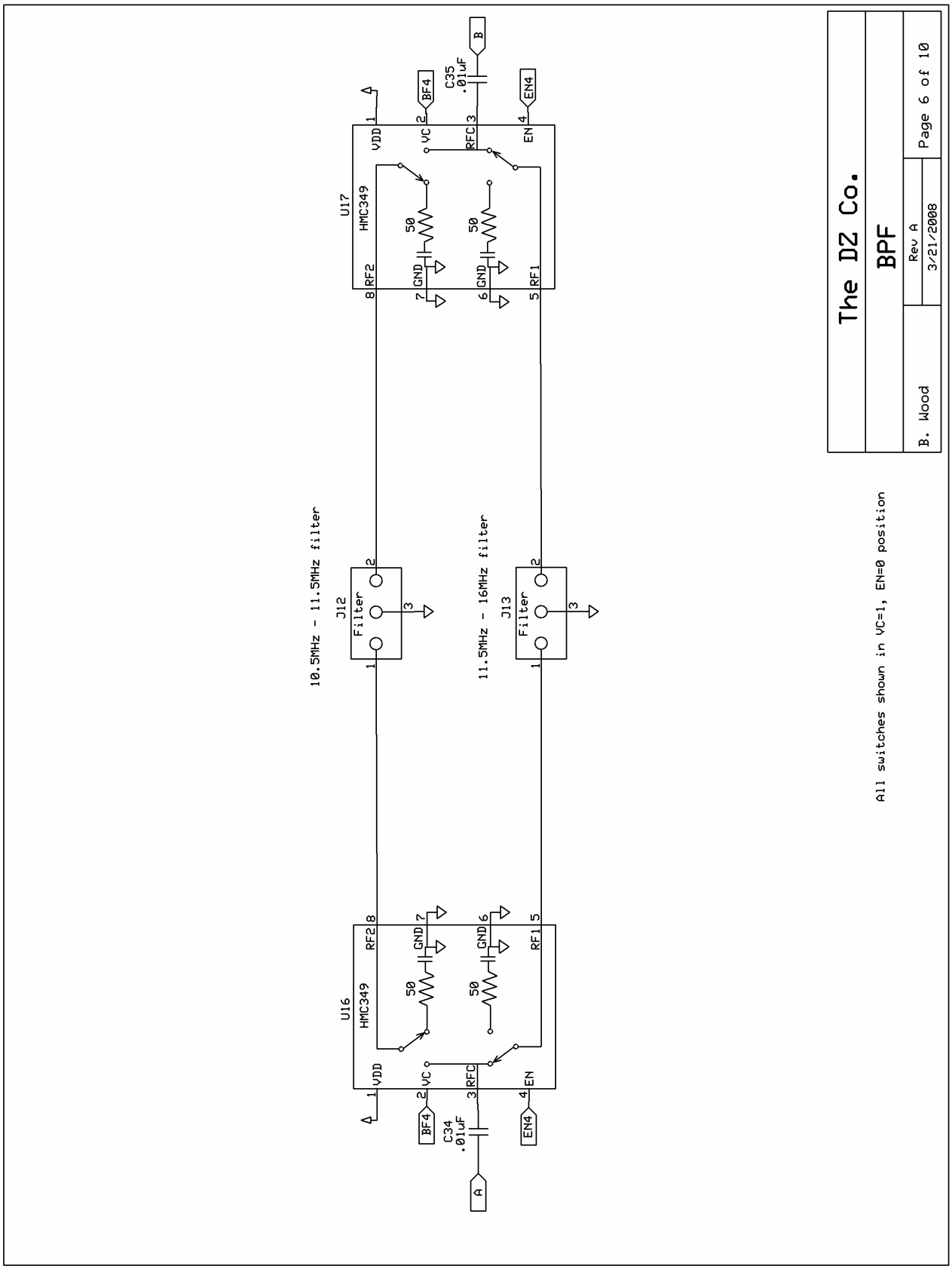
B. Wood
All switches shown in VC=1, EN=0 position
6.75MHz - 9.0MHz filter
9.0MHz - 10.5MHz filter
J10
J11
Filter
U14
U15
HMC349
VDD
VC
RFC
EN
RF1
RF2
GND
50
BF3
EN3
C32
C33
.01uF
A
B


The DZ Co.
BPF
B. Wood
Rev A
3/21/2008
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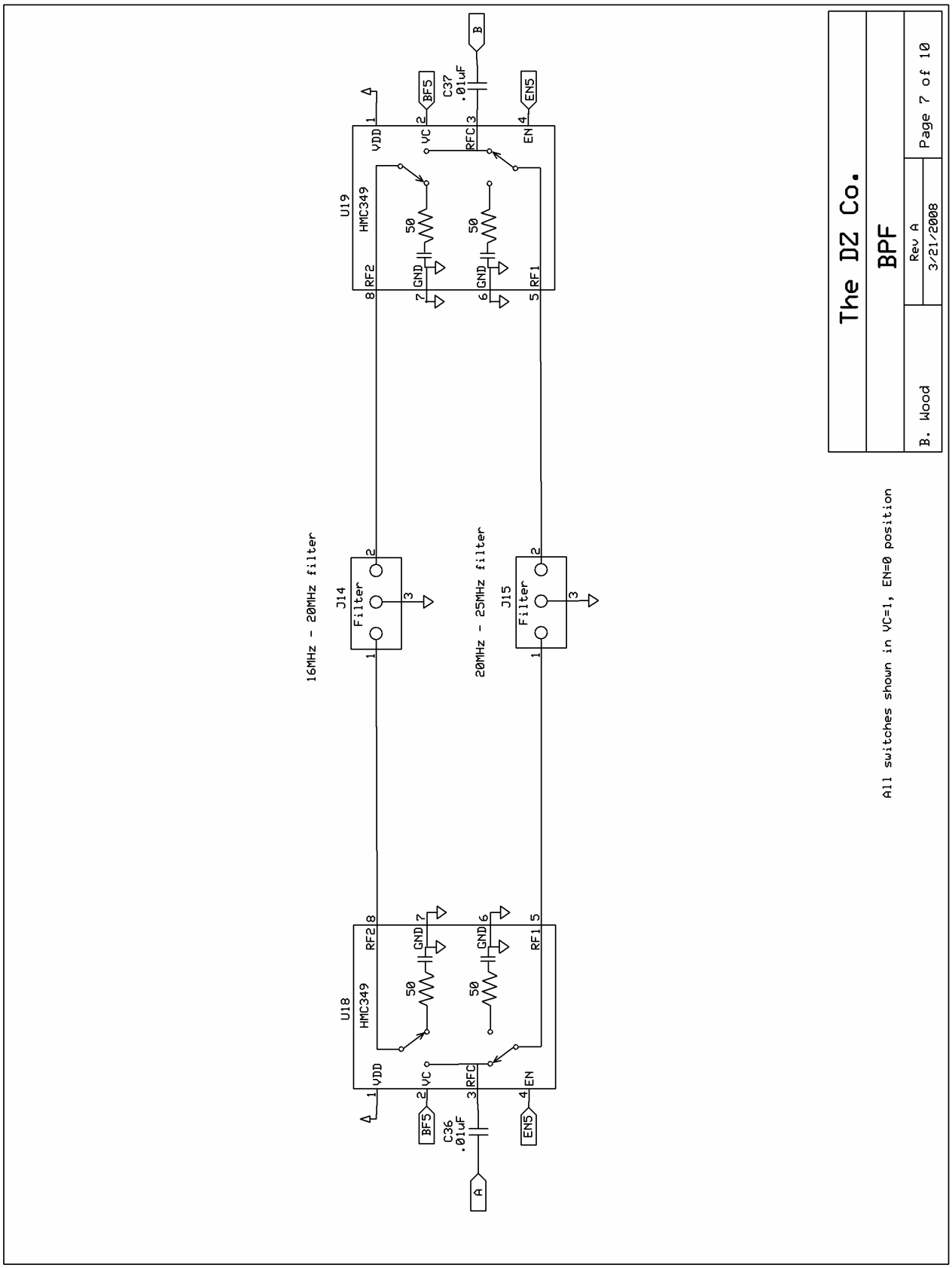
All switches shown in VC=1, EN=0 position
10.5MHz - 11.5MHz filter
11.5MHz - 16MHz filter
J12
Filter
J13
Filter
U16
HMC349
U17
HMC349
VDD
VC
RFC
EN
RF2
RF1
GND
50
BF4
EN4
A
B
C34
.01uF
C35
.01uF


The DZ Co.
BPF
B. Wood
Rev A
3/21/2008
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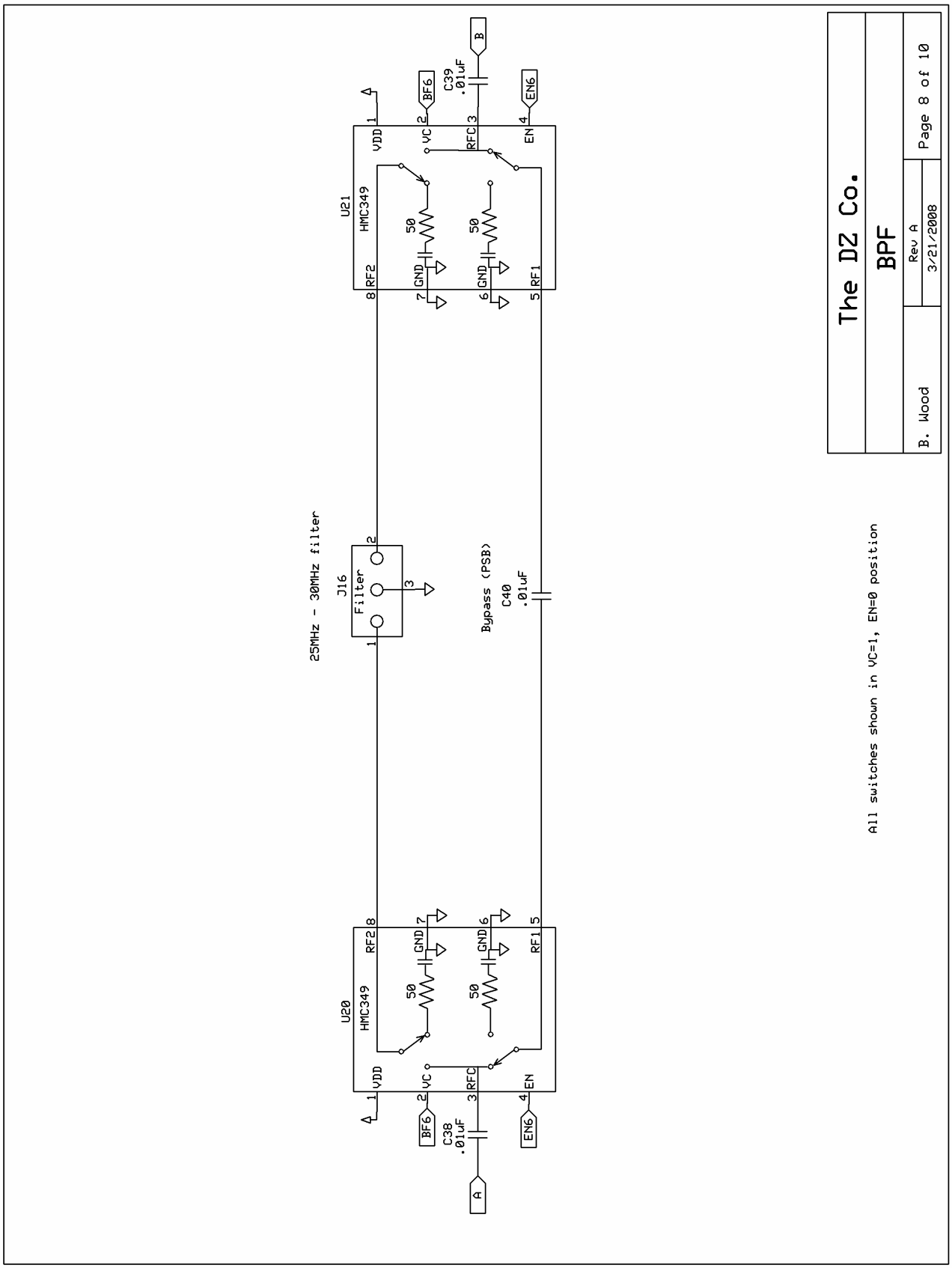
All switches shown in VC=1, EN=0 position
16MHz - 20MHz filter
20MHz - 25MHz filter
J14
J15
Filter
U18
U19
HMC349
VDD
VC
RFC
EN
RF1
RF2
GND
50
C36
.01uF
C37
.01uF
BF5
EN5
A
B


The DZ Co.
BPF
B. Wood
Rev A
3/21/2008
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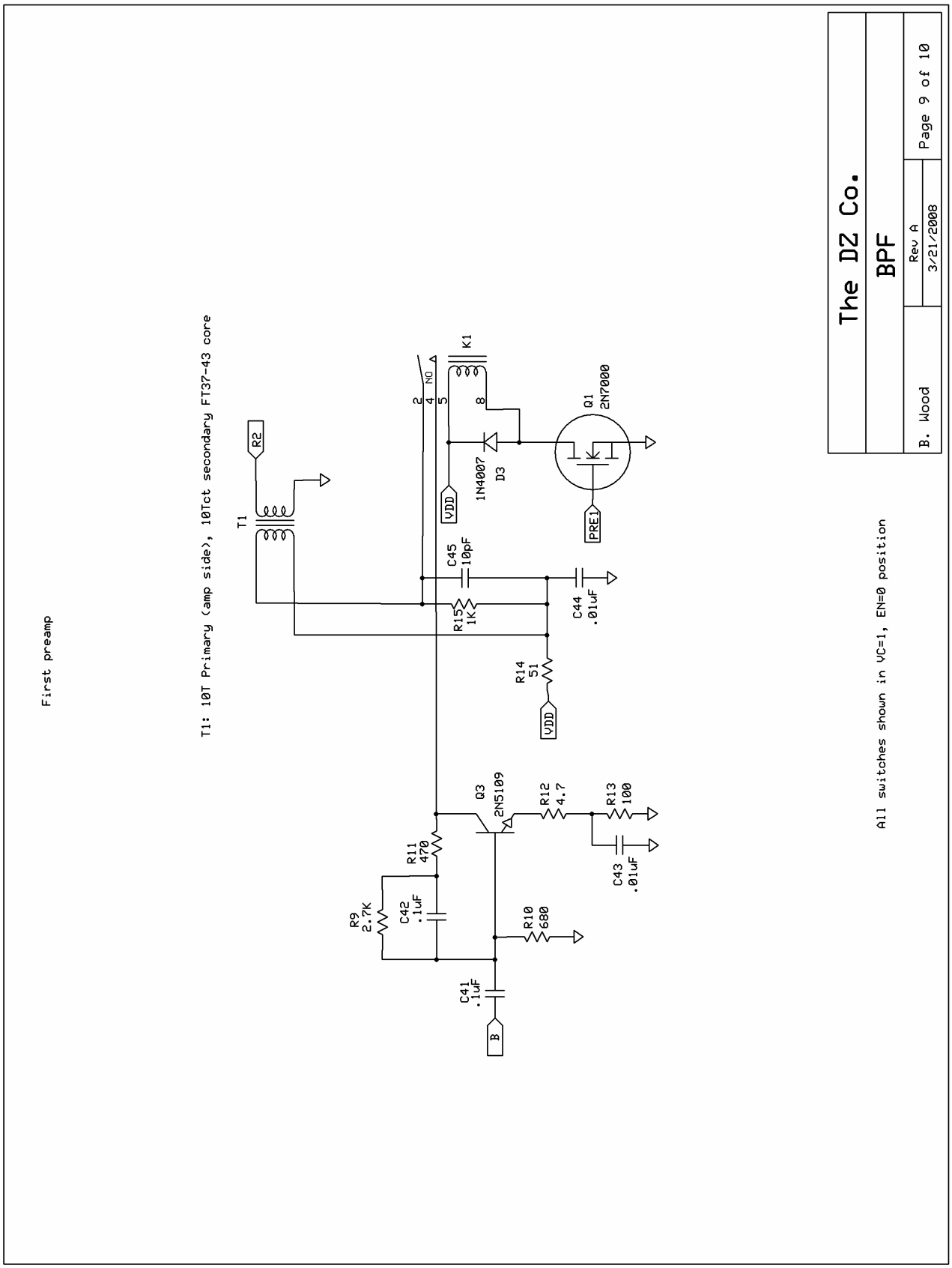
All switches shown in VC=1, EN=0 position
25MHz - 30MHz filter
J16
Filter
Bypass (PSB)
C40
.01uF
U21
HMC349
U20
HMC349
VDD
VC
RFC
EN
RF2
RF1
GND
50
C39
.01uF
C38
.01uF
BF6
EN6
A
B


First preamp
T1: 10T Primary (amp side), 10Tct secondary FT37-43 core
T1
R2
K1
2
4
5
8
NO
1N4007
D3
VDD
Q1
2N7000
PRE1
C45
10pF
R15
1K
C44
.01uF
R14
51
VDD
Q3
2N5109
R12
4.7
R13
100
C43
.01uF
R11
470
R9
2.7K
C42
.1uF
R10
680
C41
.1uF
B
All switches shown in VC=1, EN=0 position
The DZ Co.
BPF
B. Wood
Rev A
3/21/2008
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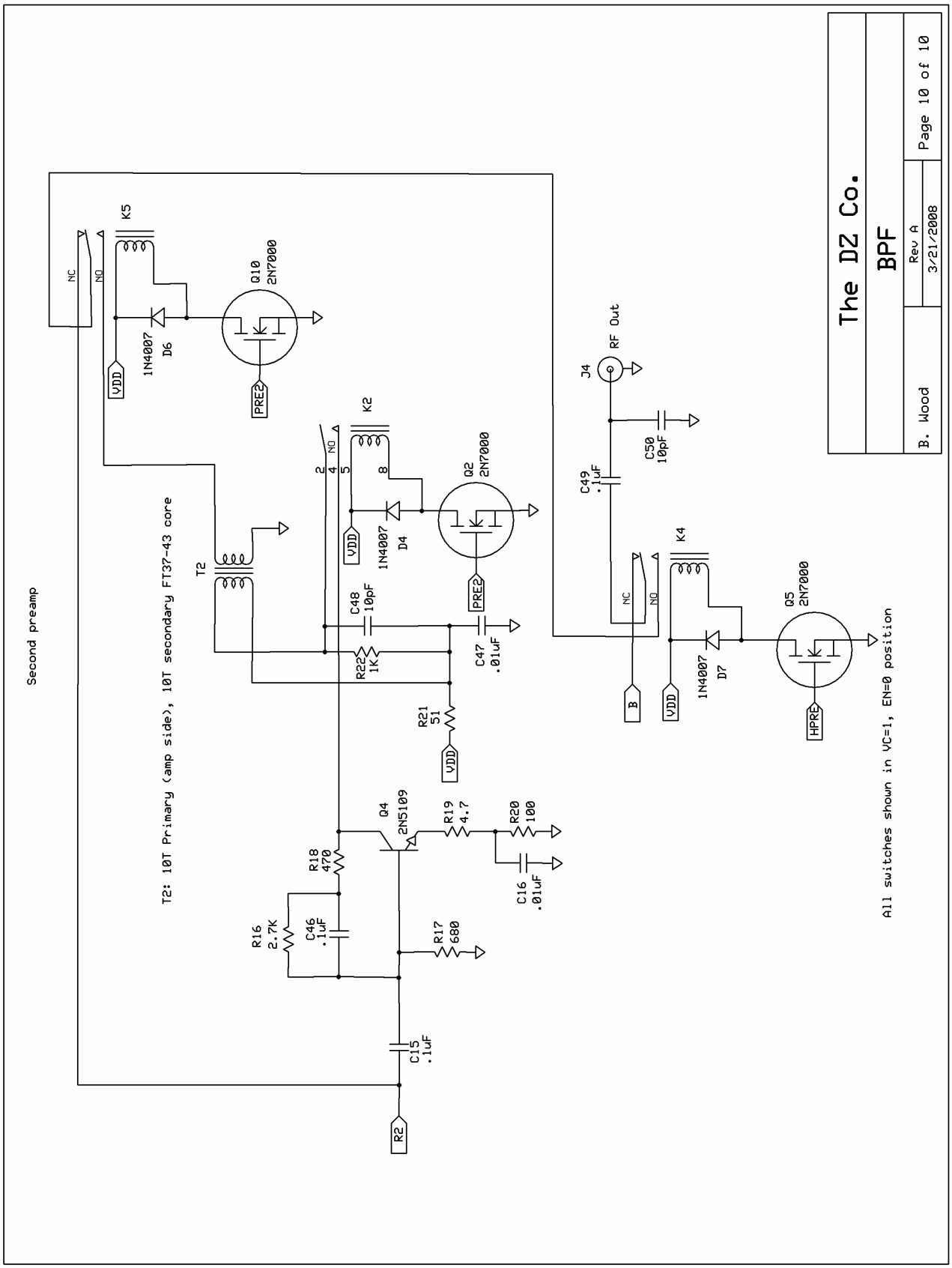
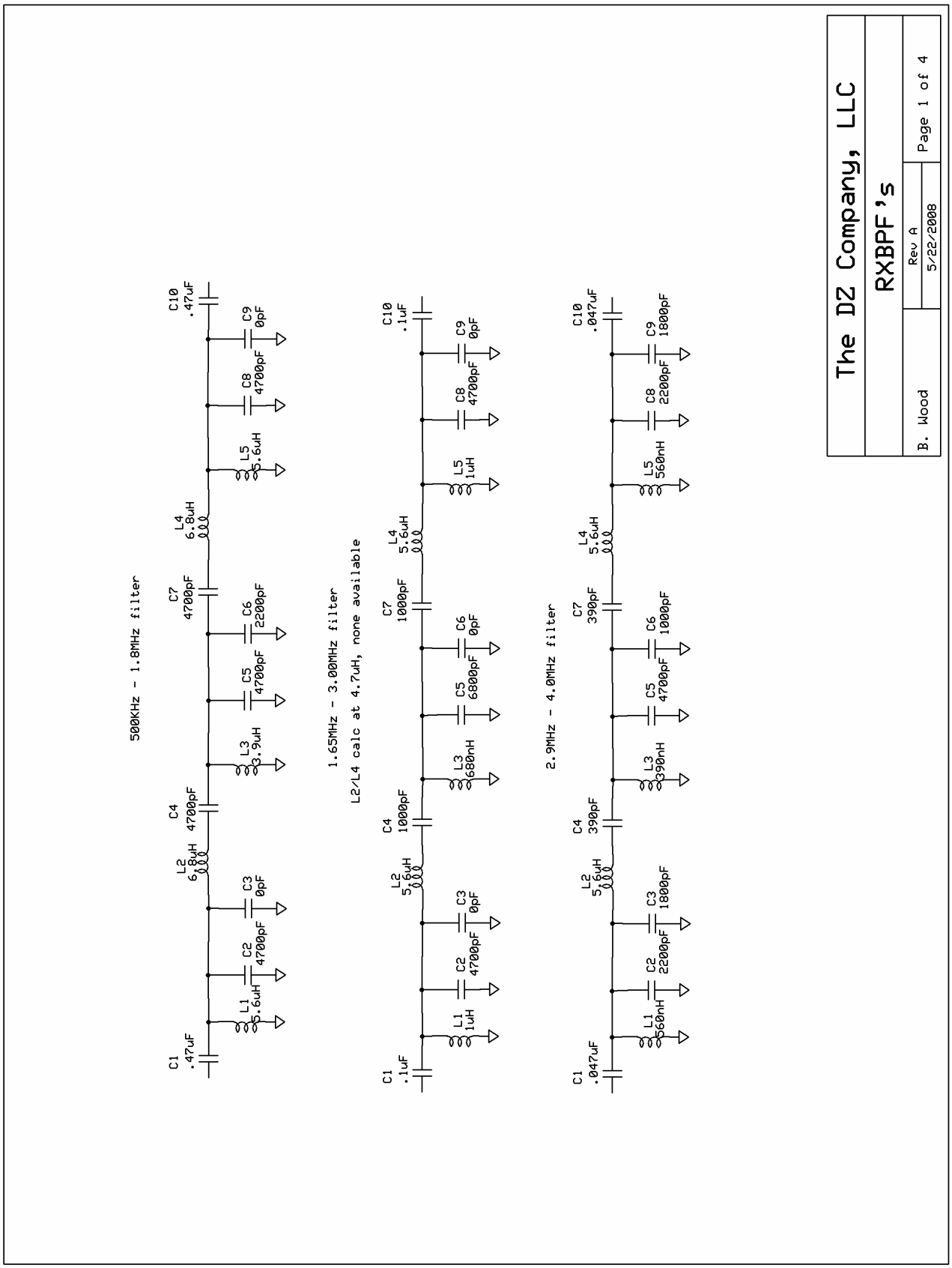

The DZ Co.
BPF
Rev A
3/21/2008
Page 10 of 10
B. Wood
Second preamp
T2: 10T Primary (amp side), 10T secondary FT37-43 core
All switches shown in VC=1, EN=0 position
K5
K2
K4
Q10 2N7000
Q2 2N7000
Q5 2N7000
Q4 2N5109
D6 1N4007
D4 1N4007
D7 1N4007
T2
J4 RF Out
C50 10pF
C49 .1uF
C48 10pF
C47 .01uF
R22 1K
R21 51
R19 4.7
R20 100
C16 .01uF
R18 470
R16 2.7K
C46 .1uF
R17 680
C15 .1uF
VDD
PRE2
HPRE
R2
B
NC
NO


500KHz - 1.8MHz filter
C1 .47uF
L1 5.6uH
C2 4700pF
L2 6.8uH
C3 0pF
C4 4700pF
L3 3.9uH
C5 4700pF
C6 2200pF
C7 4700pF
L4 6.8uH
L5 5.6uH
C8 4700pF
C9 0pF
C10 .47uF
1.65MHz - 3.00MHz filter
L2/L4 calc at 4.7uH, none available
C1 .1uF
L1 1uH
C2 4700pF
L2 5.6uH
C3 0pF
C4 1000pF
L3 680nH
C5 6800pF
C6 0pF
C7 1000pF
L4 5.6uH
L5 1uH
C8 4700pF
C9 0pF
C10 .1uF
2.9MHz - 4.0MHz filter
C1 .047uF
L1 560nH
C2 2200pF
L2 5.6uH
C3 1800pF
C4 390pF
L3 390nH
C5 4700pF
C6 1000pF
C7 390pF
L4 5.6uH
L5 560nH
C8 2200pF
C9 1800pF
C10 .047uF
The DZ Company, LLC
RXBPF's
B. Wood
Rev A
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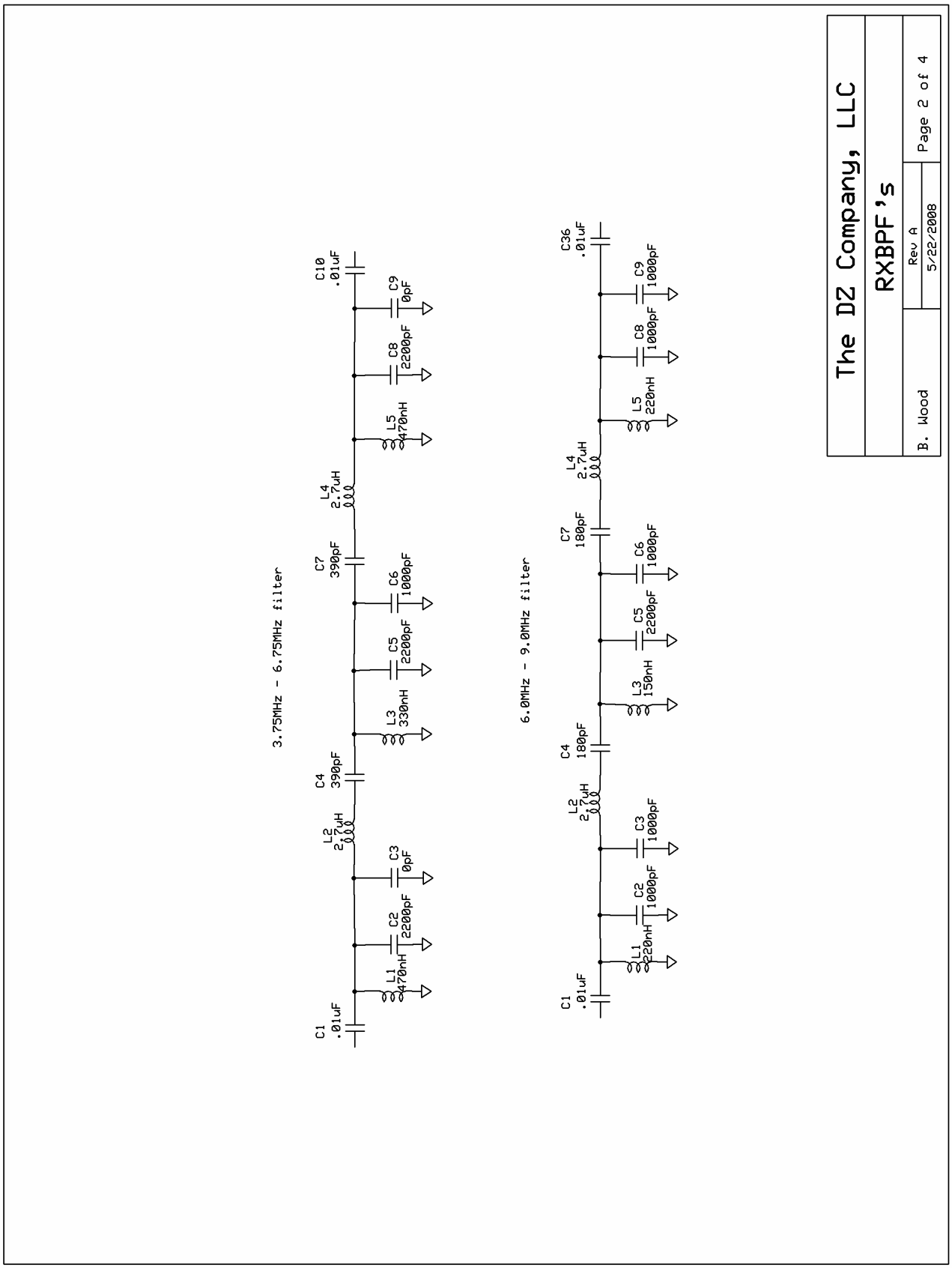
3.75MHz - 6.75MHz filter
C1 .01uF
L1 470nH
C2 2200pF
L2 2.7uH
C3 0pF
C4 390pF
L3 330nH
C5 2200pF
C6 1000pF
C7 390pF
L4 2.7uH
L5 470nH
C8 2200pF
C9 0pF
C10 .01uF
6.0MHz - 9.0MHz filter
C1 .01uF
L1 220nH
C2 1000pF
L2 2.7uH
C3 1000pF
C4 180pF
L3 150nH
C5 2200pF
C6 1000pF
C7 180pF
L4 2.7uH
L5 220nH
C8 1000pF
C9 1000pF
C36 .01uF
The DZ Company, LLC
RXBPF's
B. Wood
Rev A
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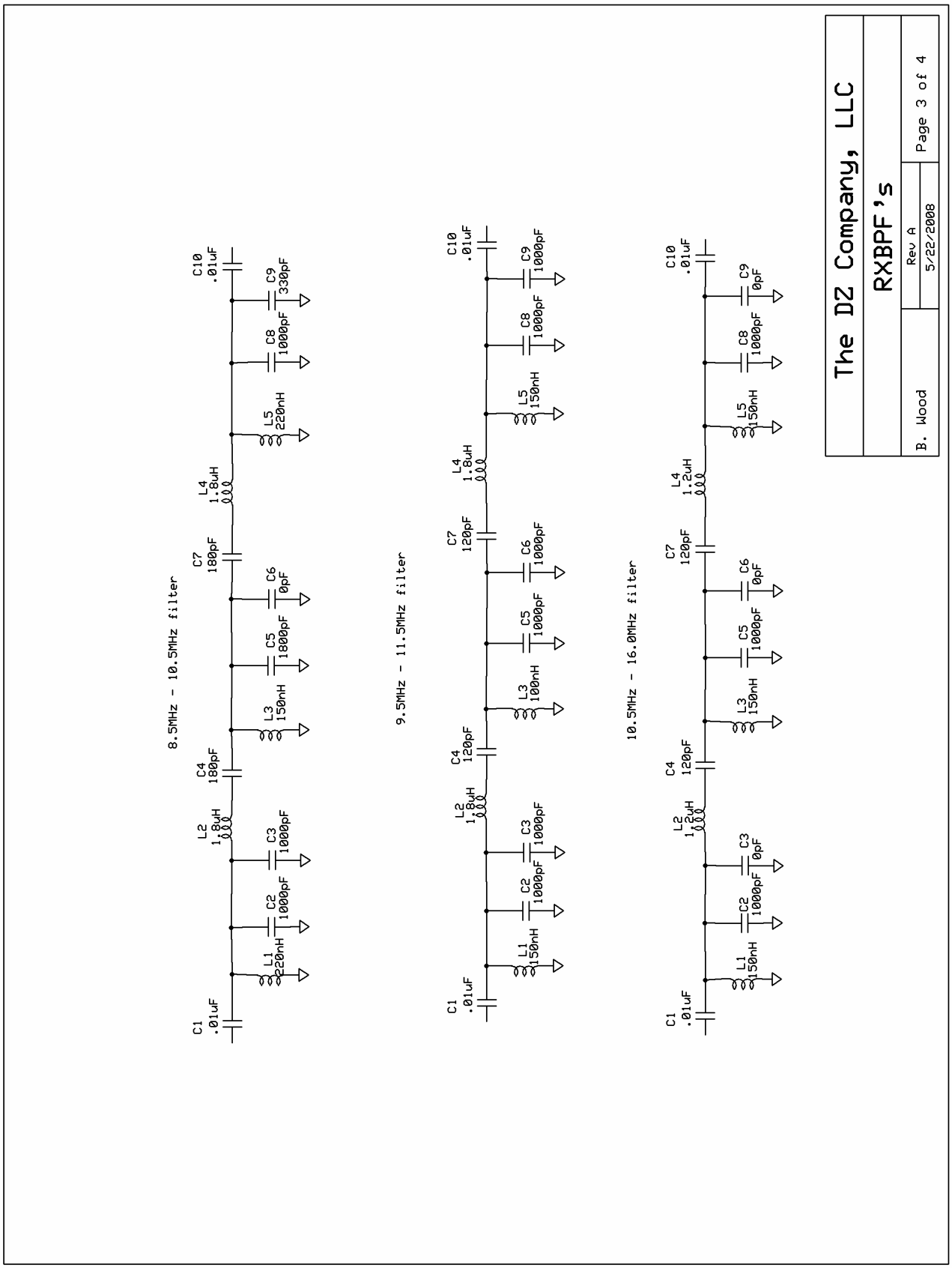
8.5MHz - 10.5MHz filter
C1 .01uF
L1 220nH
C2 1000pF
L2 1.8uH
C3 1000pF
C4 180pF
L3 150nH
C5 1800pF
C7 180pF
C6 0pF
L4 1.8uH
L5 220nH
C8 1000pF
C10 .01uF
C9 330pF
9.5MHz - 11.5MHz filter
C1 .01uF
L1 150nH
C2 1000pF
L2 1.8uH
C3 1000pF
C4 120pF
L3 100nH
C5 1000pF
C7 120pF
C6 1000pF
L4 1.8uH
L5 150nH
C8 1000pF
C10 .01uF
C9 1000pF
10.5MHz - 16.0MHz filter
C1 .01uF
L1 150nH
C2 1000pF
L2 1.2uH
C3 0pF
C4 120pF
L3 150nH
C5 1000pF
C7 120pF
C6 0pF
L4 1.2uH
L5 150nH
C8 1000pF
C10 .01uF
C9 0pF
The DZ Company, LLC
RXBPF's
B. Wood
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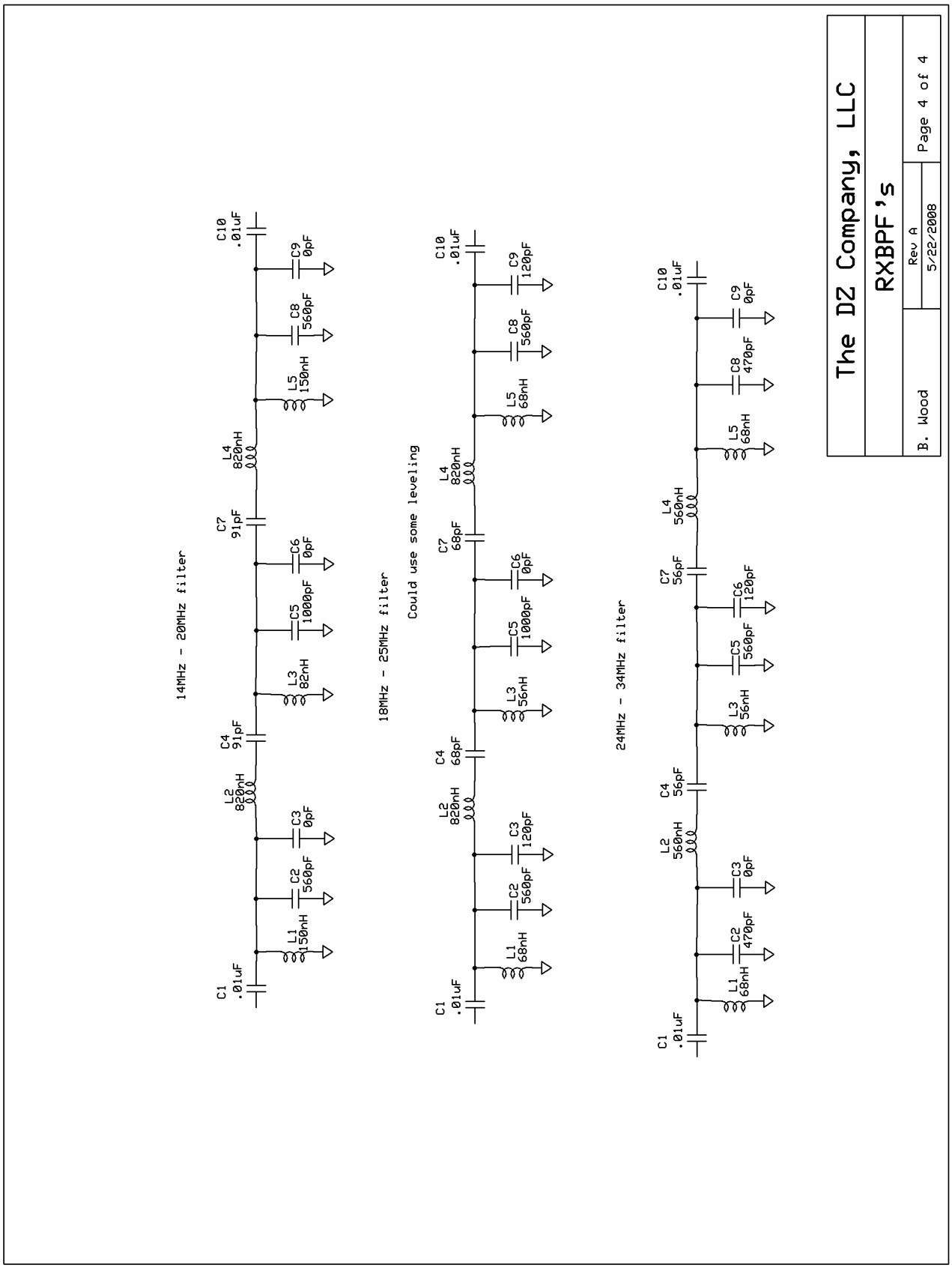
14MHz - 20MHz filter
C1 .01uF
L1 150nH
C2 560pF
C3 0pF
L2 820nH
C4 91pF
L3 82nH
C5 1000pF
C6 0pF
C7 91pF
L4 820nH
L5 150nH
C8 560pF
C9 0pF
C10 .01uF
18MHz - 25MHz filter
Could use some leveling
C1 .01uF
L1 68nH
C2 560pF
C3 120pF
L2 820nH
C4 68pF
L3 56nH
C5 1000pF
C6 0pF
C7 68pF
L4 820nH
L5 68nH
C8 560pF
C9 120pF
C10 .01uF
24MHz - 34MHz filter
C1 .01uF
L1 68nH
C2 470pF
C3 0pF
L2 560nH
C4 56pF
L3 56nH
C5 560pF
C6 120pF
C7 56pF
L4 560nH
L5 68nH
C8 470pF
C9 0pF
C10 .01uF
The DZ Company, LLC
RXBPF's
B. Wood
Rev A
5/22/2008
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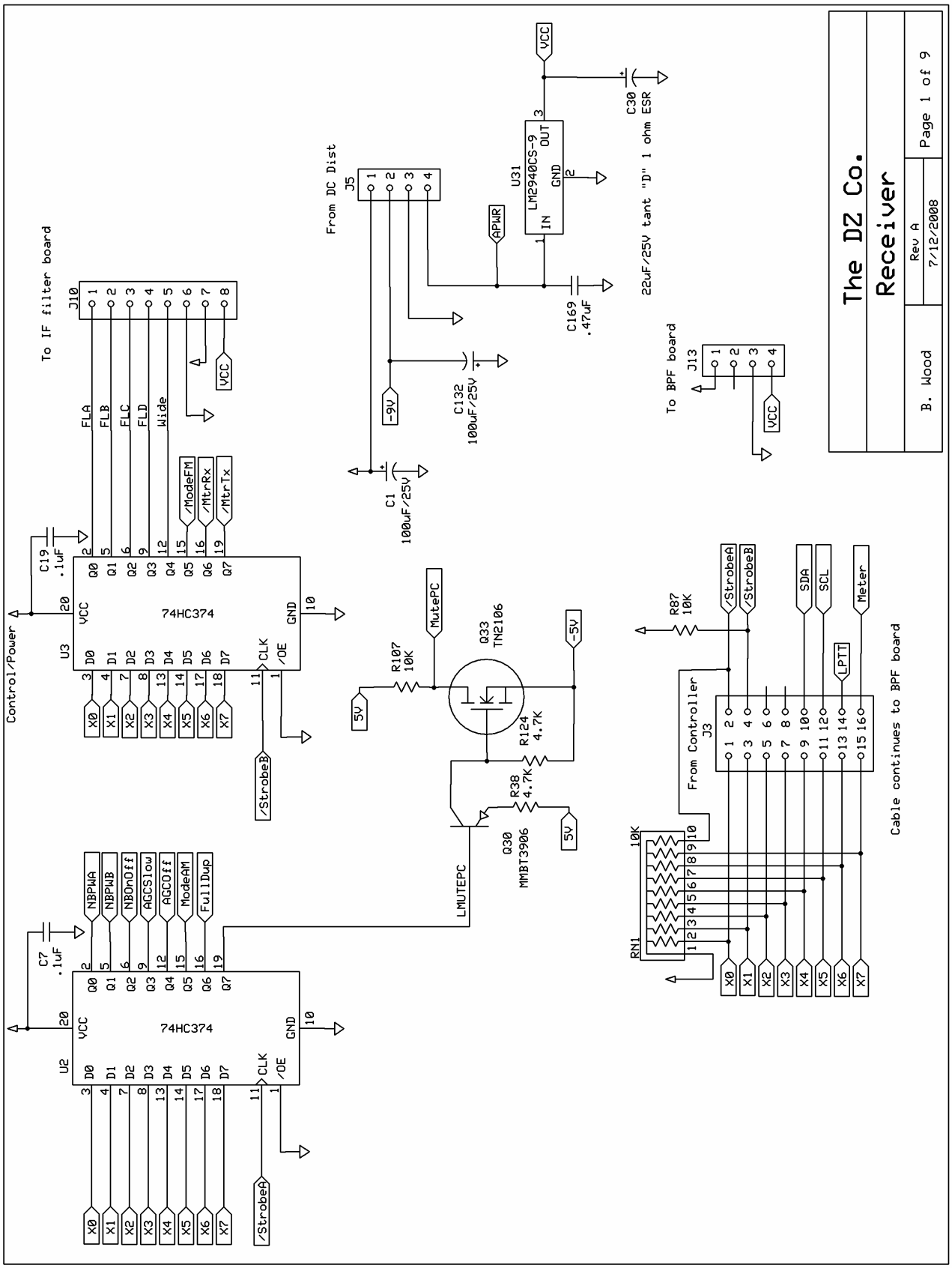
The DZ Co.
Receiver
B. Wood
Rev A
7/12/2008
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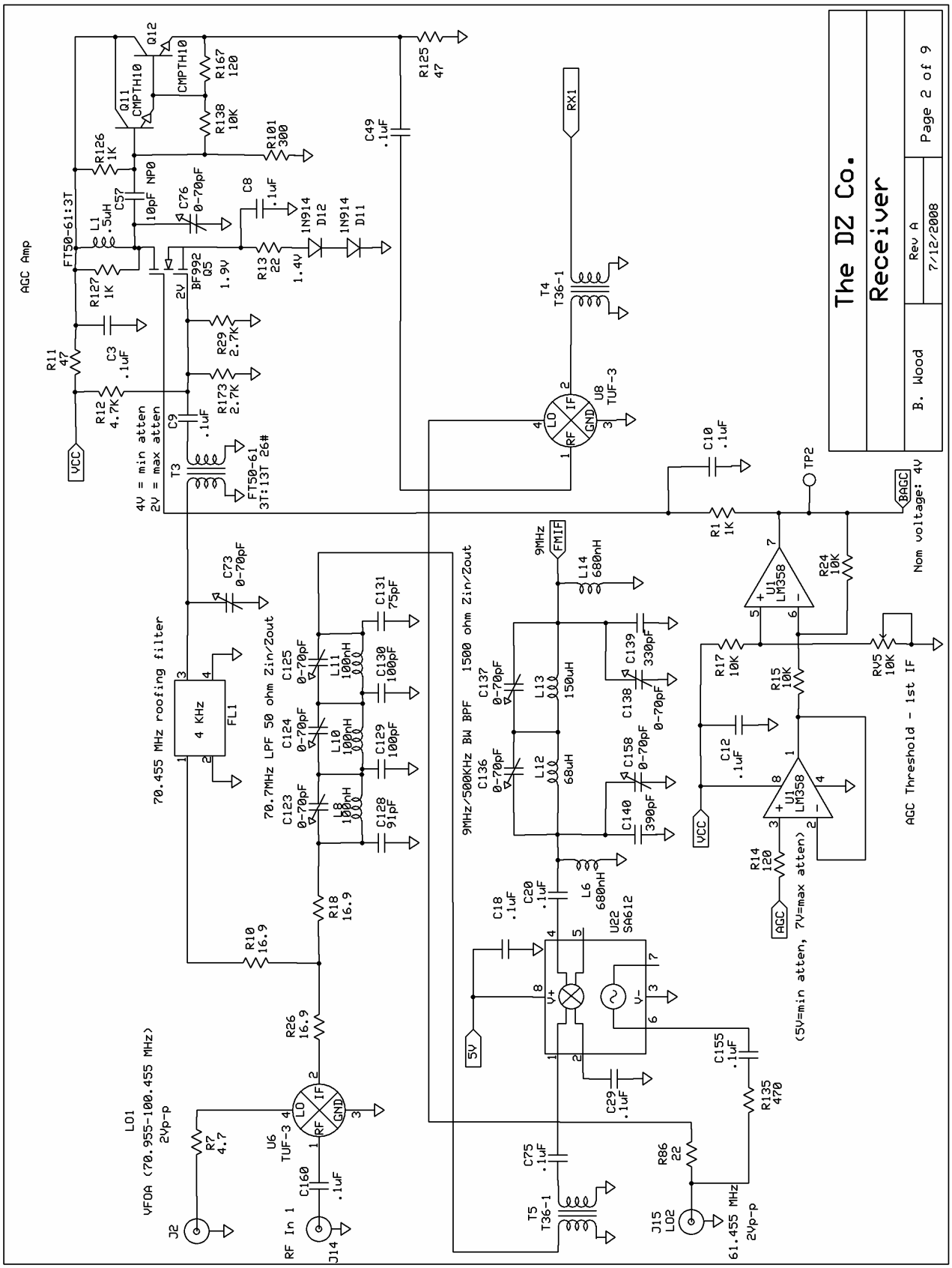
To IF filter board
From DC Dist
To BPF board
Control/Power
From Controller
Cable continues to BPF board
74HC374
U2
U3
J10
J5
J13
J3
U31
LM2940CS-9
C1
100uF/25V
C132
100uF/25V
C169
.47uF
C30
22uF/25V tant "D" 1 ohm ESR
C7
.1uF
C19
.1uF
R87
10K
R107
10K
R124
4.7K
R38
4.7K
RN1
10K
Q33
TN2106
Q30
MMBT3906
APWR
-9V
5V
-5V
VCC
MutePC
LMUTEPC
/StrobeA
/StrobeB
/ModeFM
/MtrRx
/MtrTx
NBPWA
NBPWB
NBOnOff
AGCSlow
AGCOff
ModeAM
FullDup
FLA
FLB
FLC
FLD
Wide
SDA
SCL
LPTT
Meter
X0
X1
X2
X3
X4
X5
X6
X7


The DZ Co.
Receiver
B. Wood
Rev A
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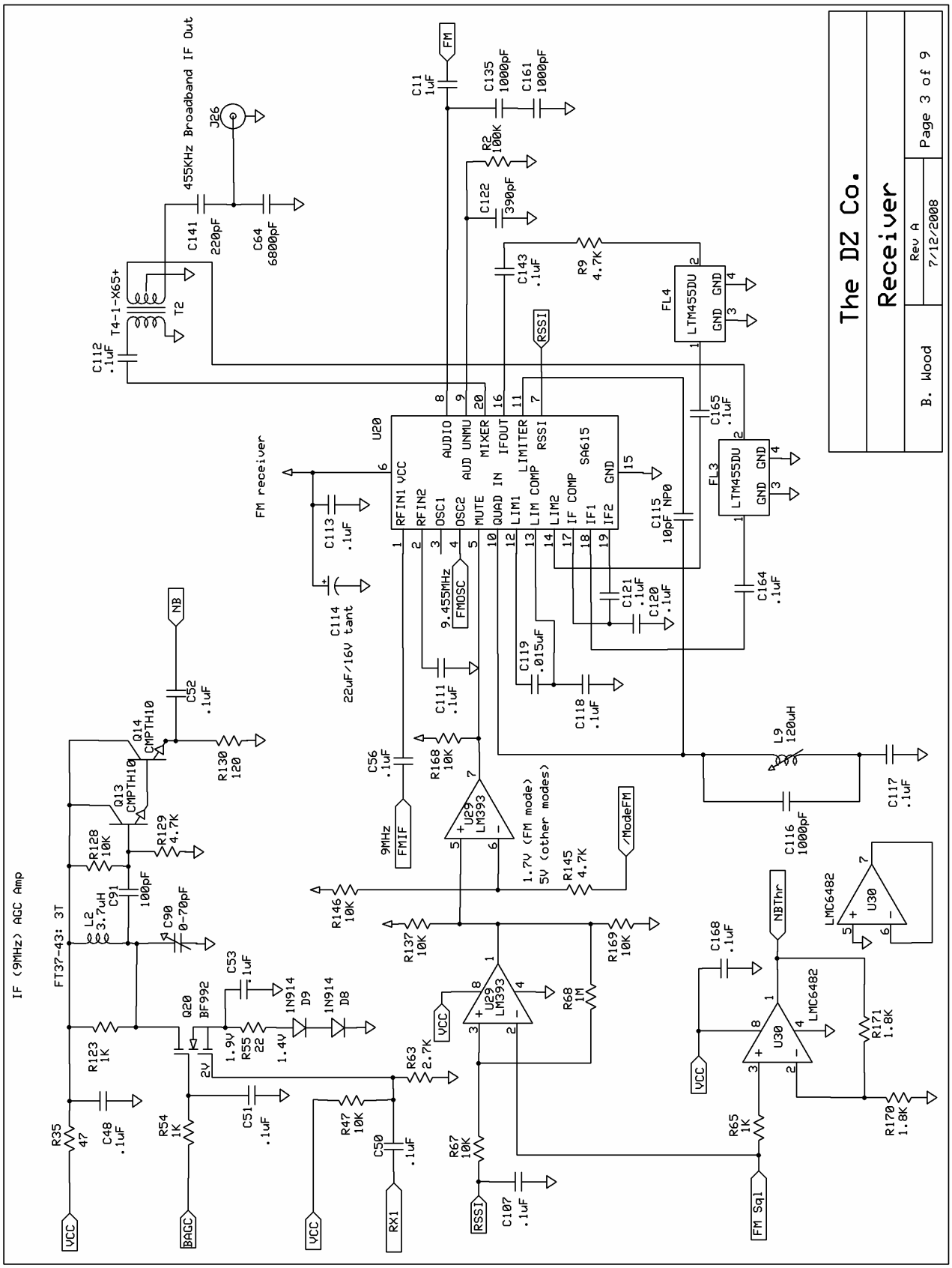
AGC Amp
4V = min atten
2V = max atten
70.455 MHz roofing filter
70.7MHz LPF 50 ohm Zin/Zout
9MHz/500KHz BW BPF 1500 ohm Zin/Zout
AGC Threshold - 1st IF
(5V=min atten, 7V=max atten)
Nom voltage: 4V
VFOA (70.955-100.455 MHz)
2Vp-p
RF In 1
61.455 MHz
2Vp-p
LO1
LO2
RX1
TP2
VCC
5V
AGC
BAGC
FMIF
9MHz
4 KHz
FL1
FT50-61:3T
FT50-61
3T:13T 26#
T3
T4
T5
T36-1
U1
LM358
U6
U8
TUF-3
U22
SA612
BF992
CMPTH10
1N914
Q5
Q11
Q12
D11
D12
J2
J14
J15
R1
R10
R11
R12
R13
R14
R15
R17
R18
R24
R26
R29
R86
R101
R125
R126
R127
R135
R138
R167
R173
RV5
C3
C8
C9
C10
C12
C18
C20
C29
C49
C57
C73
C75
C76
C123
C124
C125
C128
C129
C130
C131
C136
C137
C138
C139
C140
C155
C158
C160
L1
L6
L8
L10
L11
L12
L13
L14
RF
IF
LO
GND


The DZ Co.
Receiver
B. Wood
Rev A
7/12/2008
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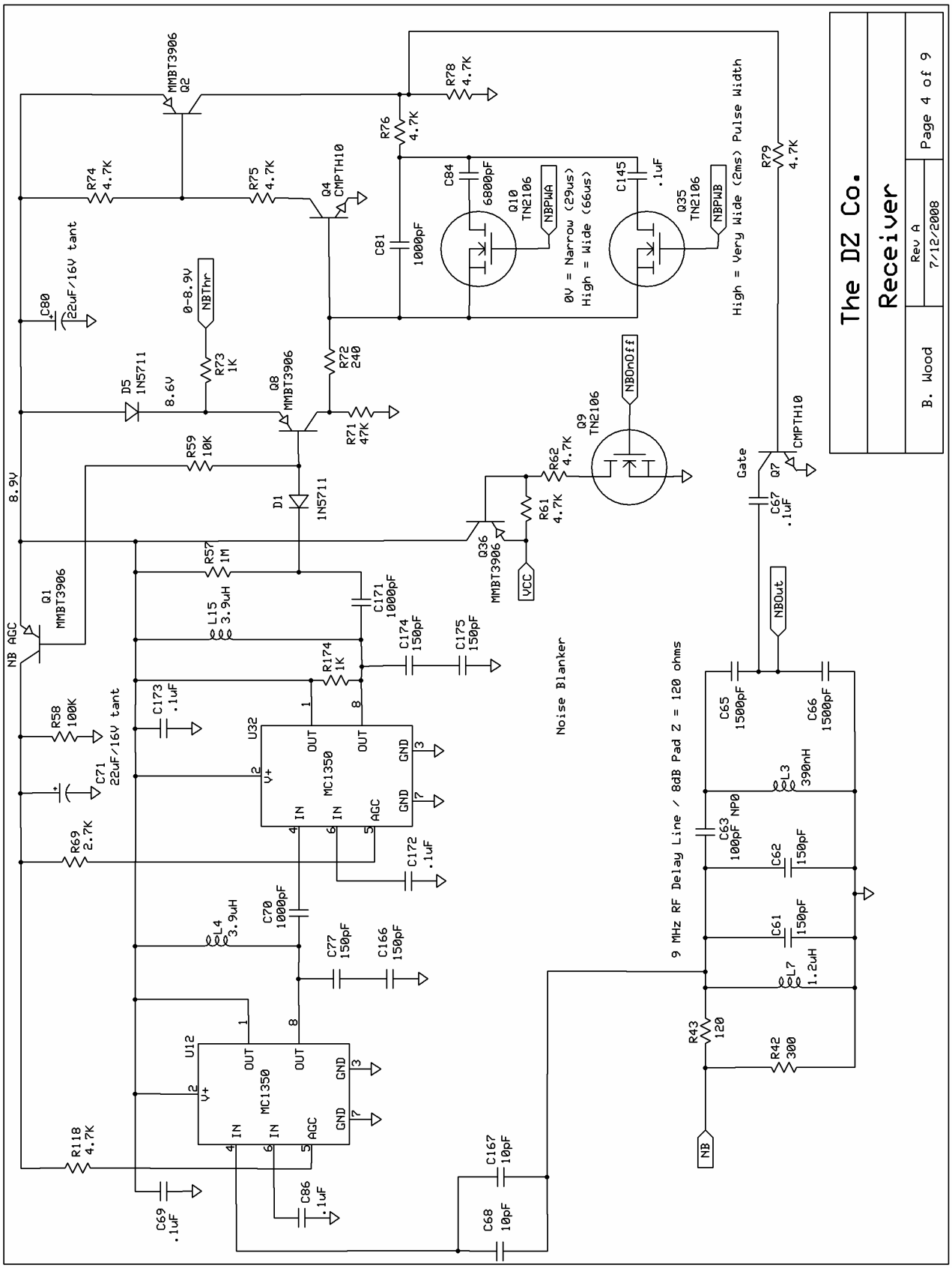
IF (9MHz) AGC Amp
FM receiver
455KHz Broadband IF Out
J26
T2
T4-1-X65+
C141 220pF
C64 6800pF
C112 .1uF
C11 1uF
FM
C135 1000pF
C161 1000pF
R2 100K
C122 390pF
C143 .1uF
R9 4.7K
RSSI
FL4 LTM455DU
C165 .1uF
FL3 LTM455DU
C164 .1uF
U20
AUDIO
AUD UNMU
MIXER
IFOUT
LIMITER
RSSI
SA615
RFIN1 VCC
RFIN2
OSC1
OSC2
MUTE
QUAD IN
LIM1
LIM COMP
LIM2
IF COMP
IF1
IF2
GND
C113 .1uF
C114 22uF/16V tant
9.455MHz FMOSC
C111 .1uF
C115 10pF NP0
C121 .1uF
C120 .1uF
C119 .015uF
C118 .1uF
L9 120uH
C117 .1uF
C116 1000pF
NB
C52 .1uF
Q14 CMPTH10
Q13 CMPTH10
R130 120
R129 4.7K
R128 10K
C91 100pF
C90 0-70pF
L2 3.7uH
FT37-43: 3T
C56 .1uF
R168 10K
9MHz FMIF
U29 LM393
1.7V (FM mode)
5V (other modes)
/ModeFM
R145 4.7K
R146 10K
R137 10K
R169 10K
C168 .1uF
NBThr
LMC6482
U30
R171 1.8K
R170 1.8K
R65 1K
FM Sq1
R68 1M
R67 10K
C107 .1uF
RSSI
R63 2.7K
C53 .1uF
1N914 D9
1N914 D8
Q20 BF992
1.9V
1.4V
R55 22
2V
R123 1K
R35 47
C48 .1uF
R54 1K
C51 .1uF
R47 10K
C50 .1uF
VCC
BAGC
RX1


The DZ Co.
Receiver
B. Wood
Rev A
7/12/2008
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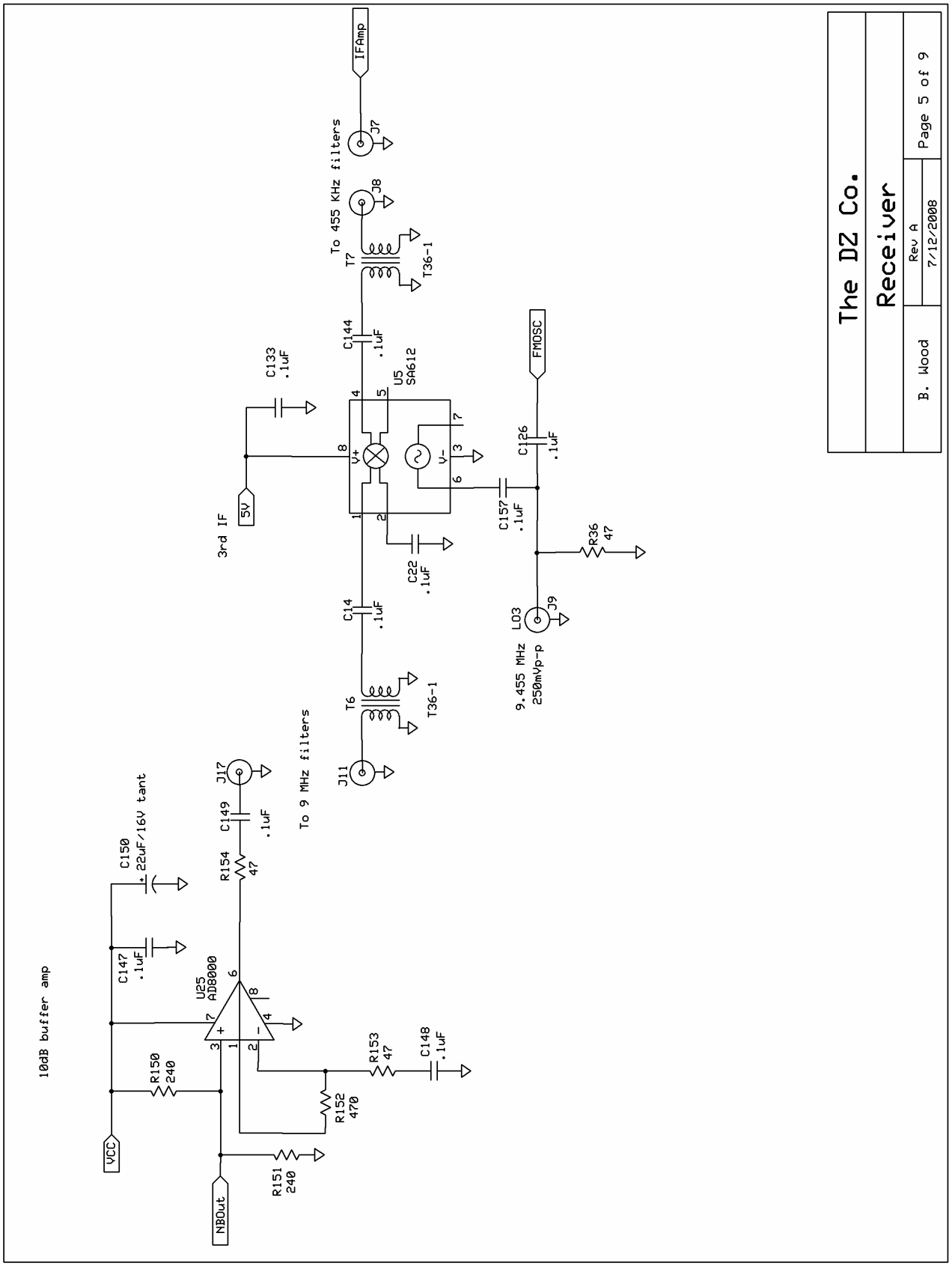
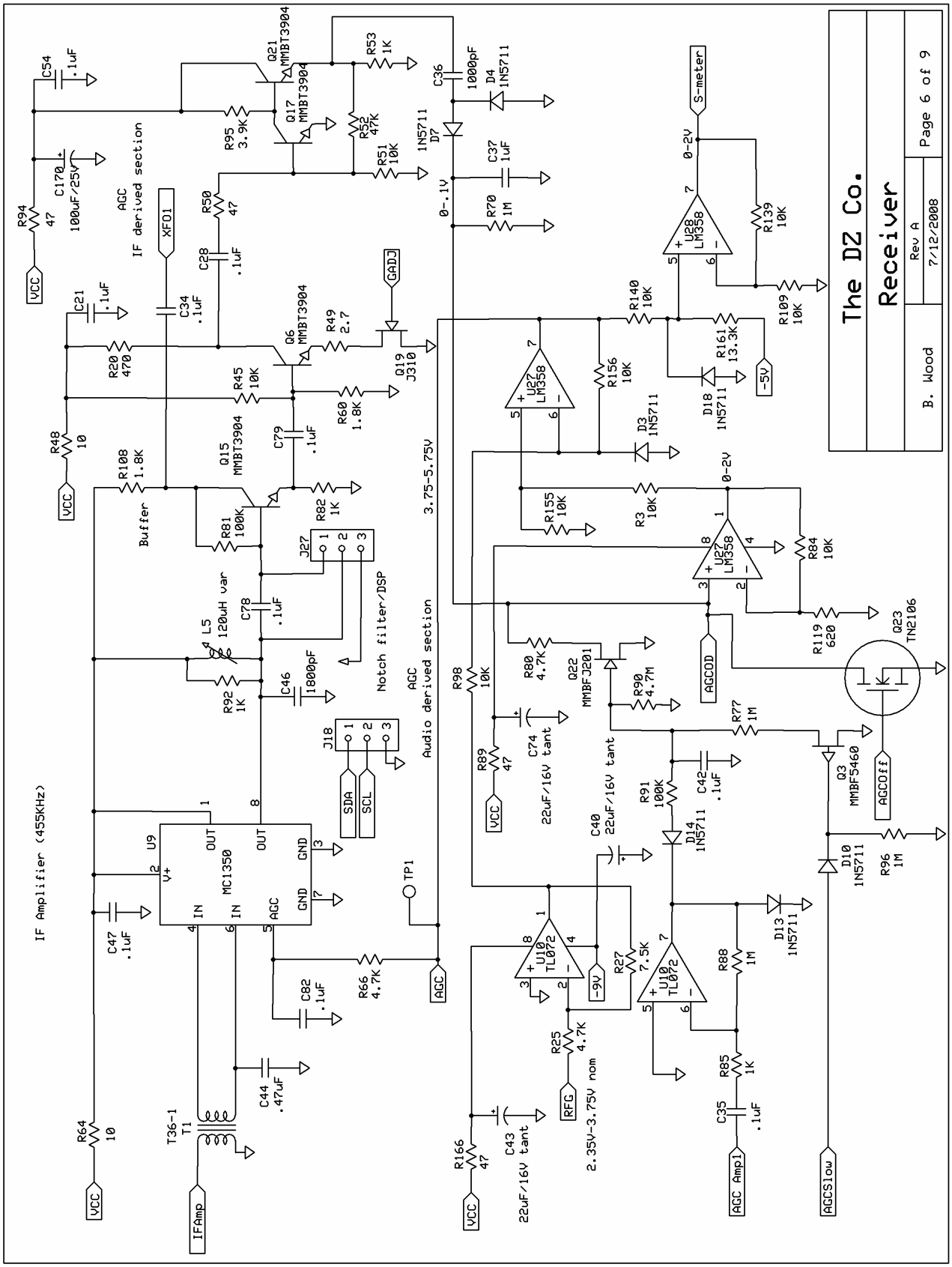
Noise Blanker
9 MHz RF Delay Line / 8dB Pad Z = 120 ohms
0V = Narrow (29us)
High = Wide (66us)
High = Very Wide (2ms) Pulse Width
MC1350
MMBT3906
CMPTH10
TN2106
1N5711
NB AGC
Gate
8.9V
VCC
NB
NBOut
NBOnOff
NBPWA
NBPWB
NBThr


The DZ Co.
Receiver
B. Wood
Rev A
7/12/2008
Page 5 of 9
10dB buffer amp
VCC
NBOut
R150 240
R151 240
R152 470
R153 47
R154 47
C147 .1uF
C150 + 22uF/16V tant
C148 .1uF
C149 .1uF
U25 AD8000
To 9 MHz filters
J11
J12
T6
T36-1
C14 .1uF
C22 .1uF
3rd IF
5V
C133 .1uF
U5 SA612
C144 .1uF
T7
T36-1
To 455 KHz filters
J8
J7
IFAmp
C157 .1uF
C126 .1uF
FMOSC
LO3
J9
9.455 MHz 250mVp-p
R36 47


The DZ Co.
Receiver
Rev A
7/12/2008
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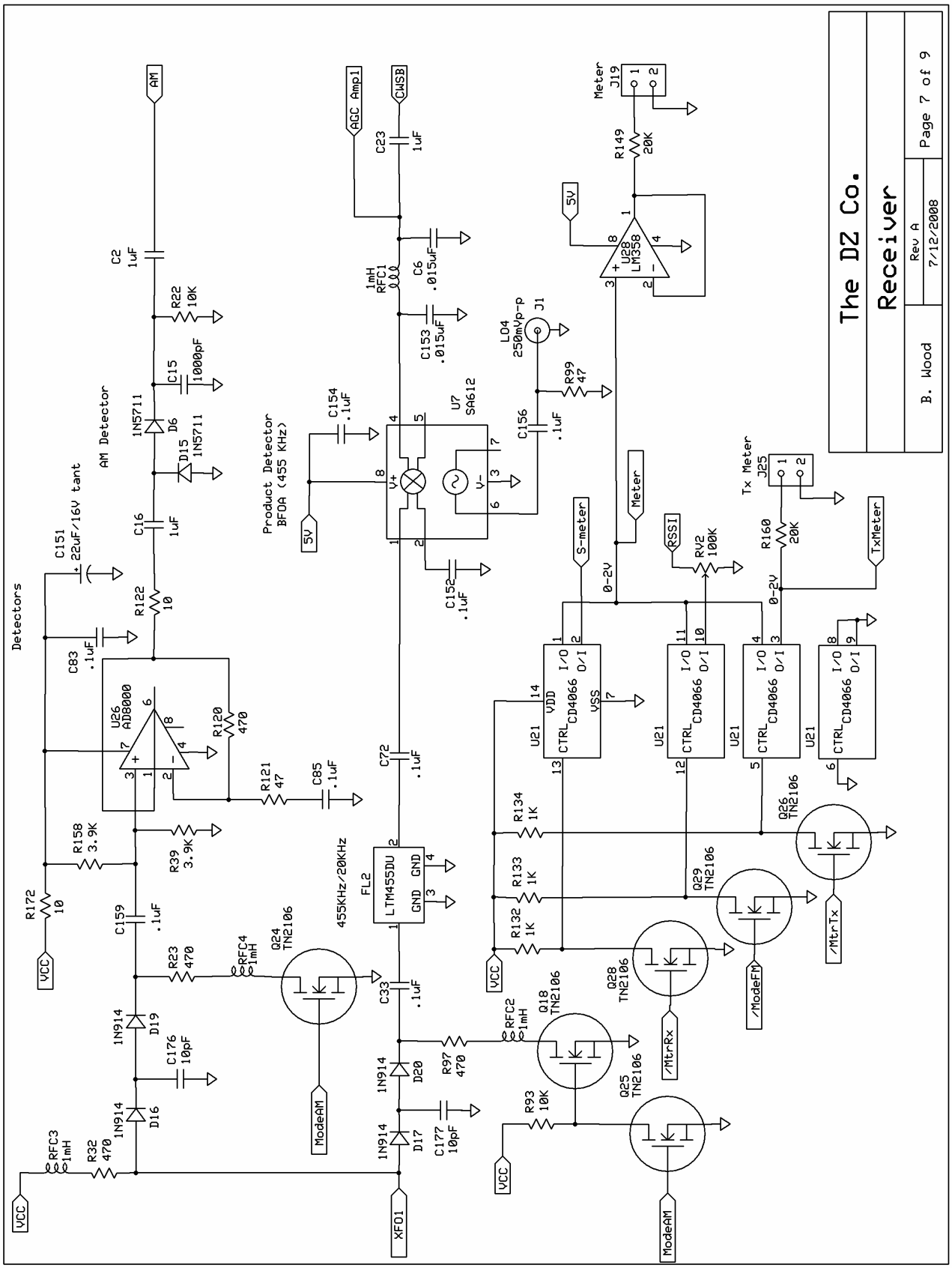
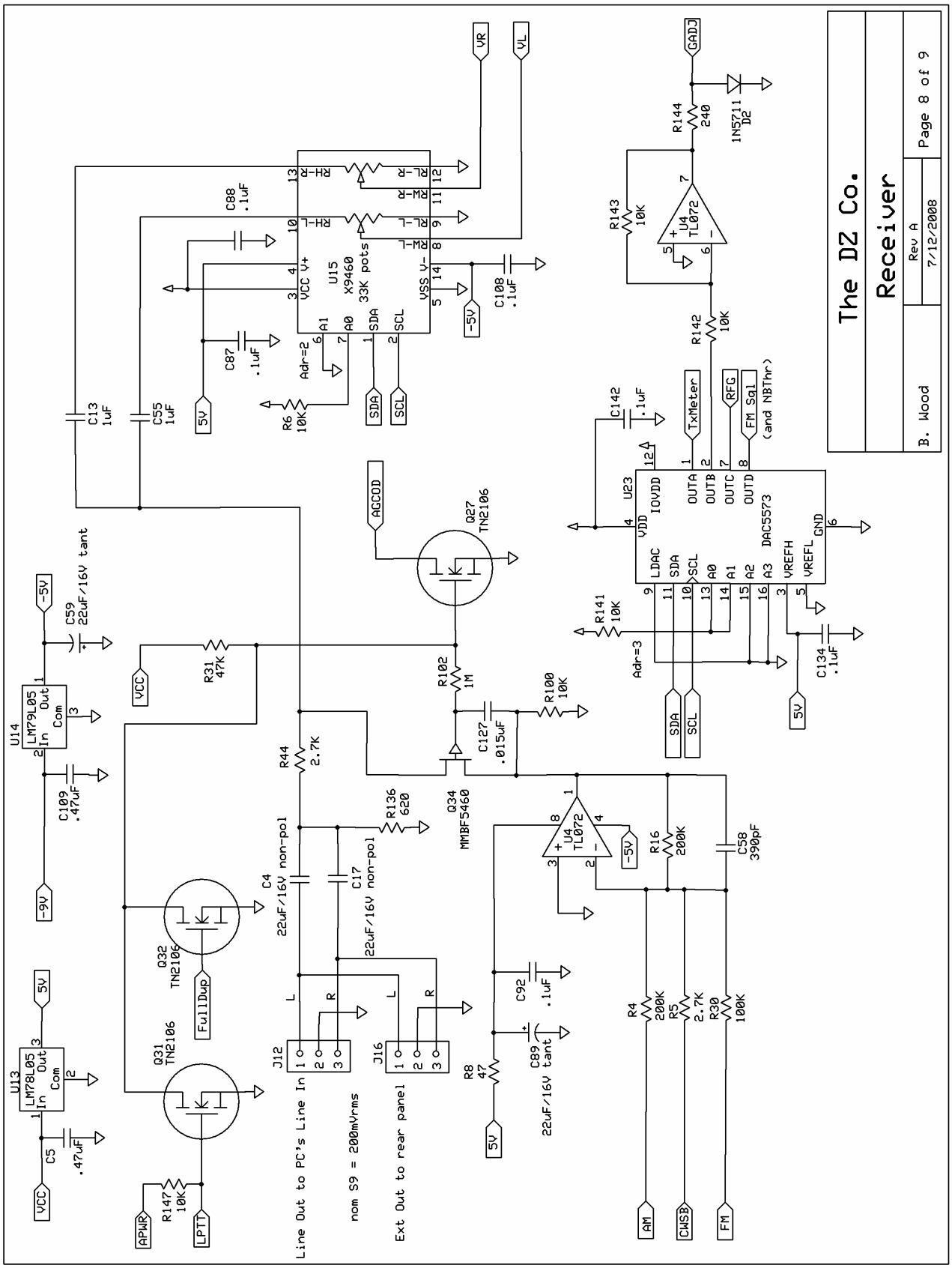
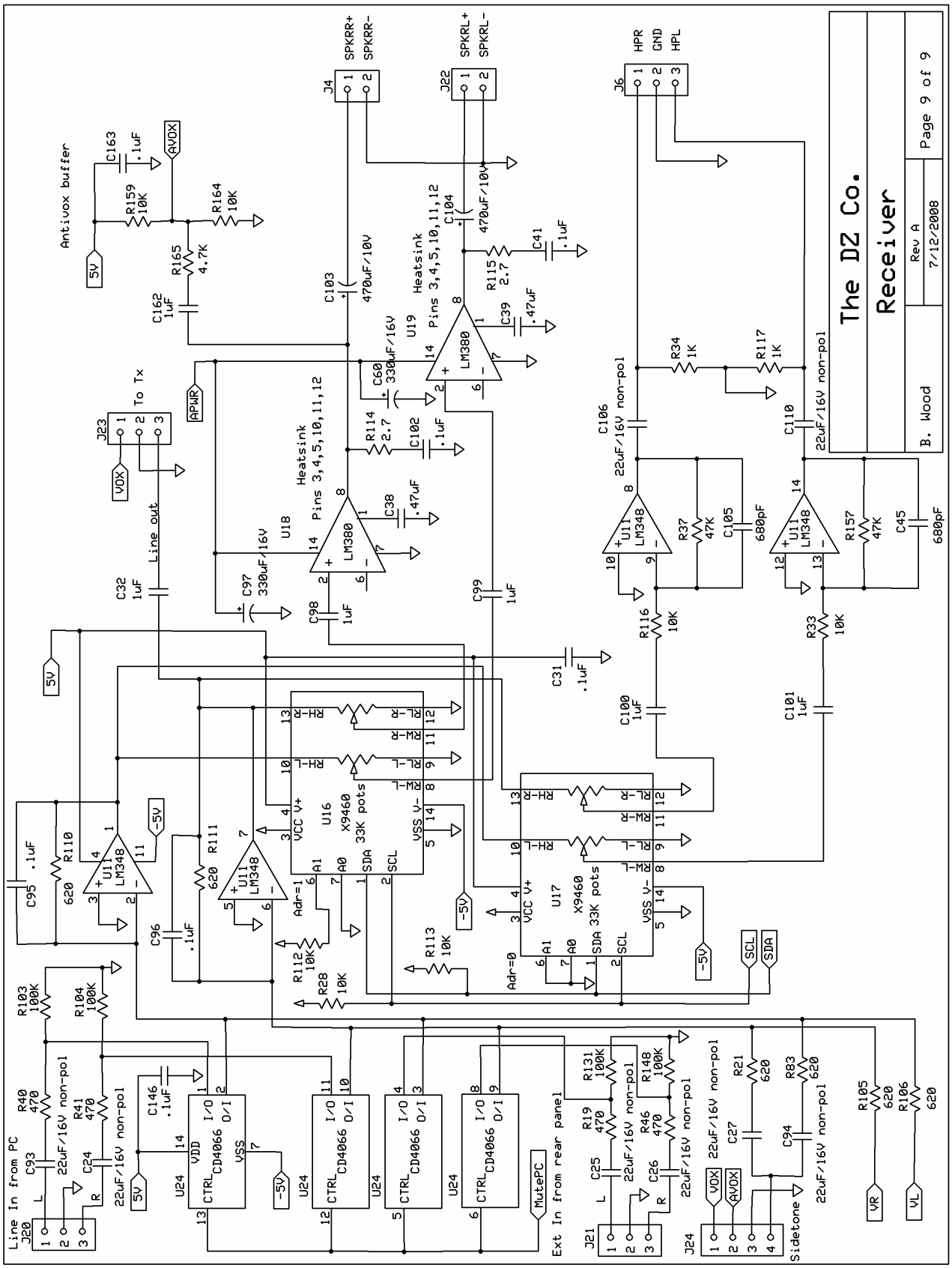
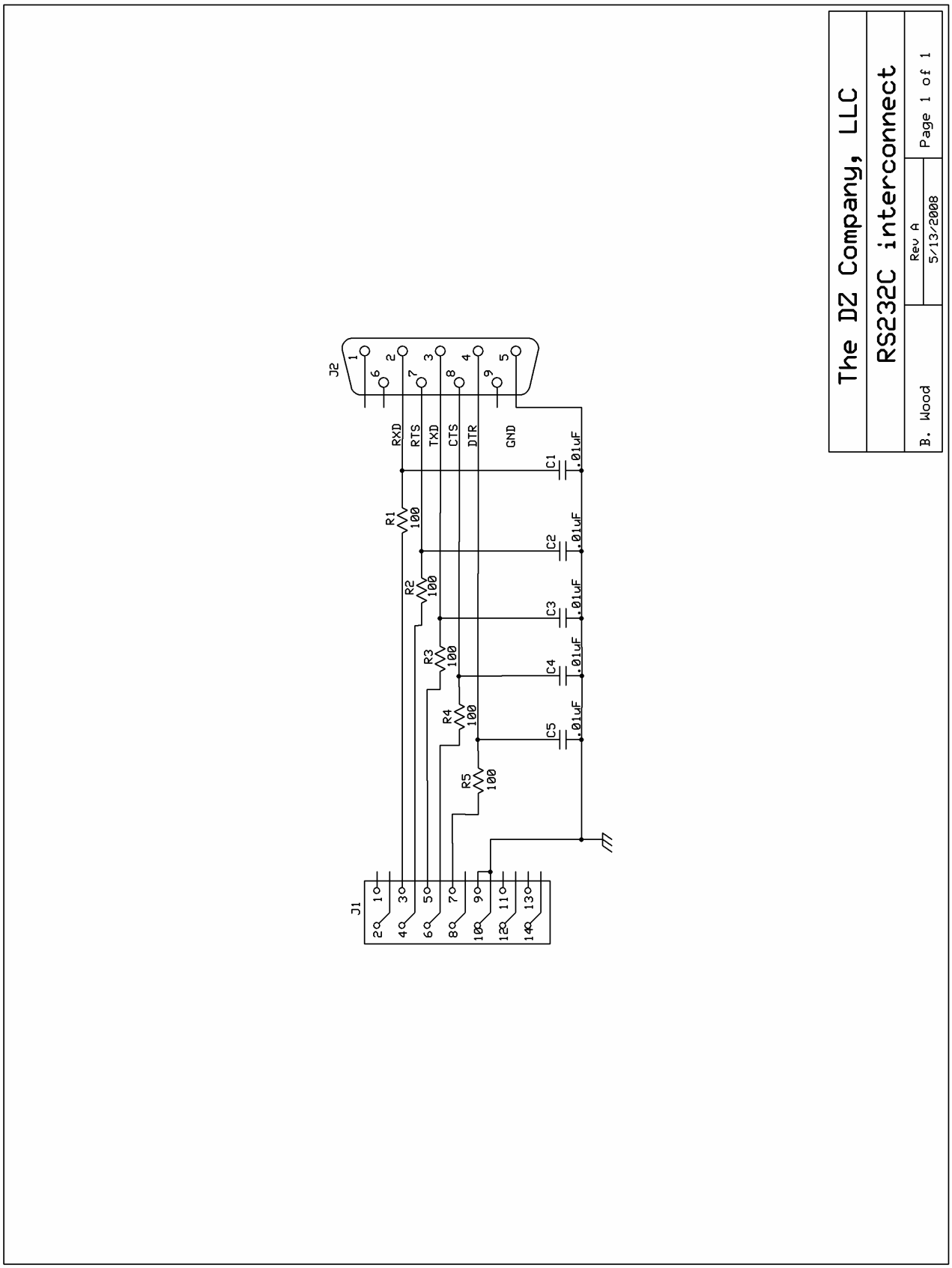
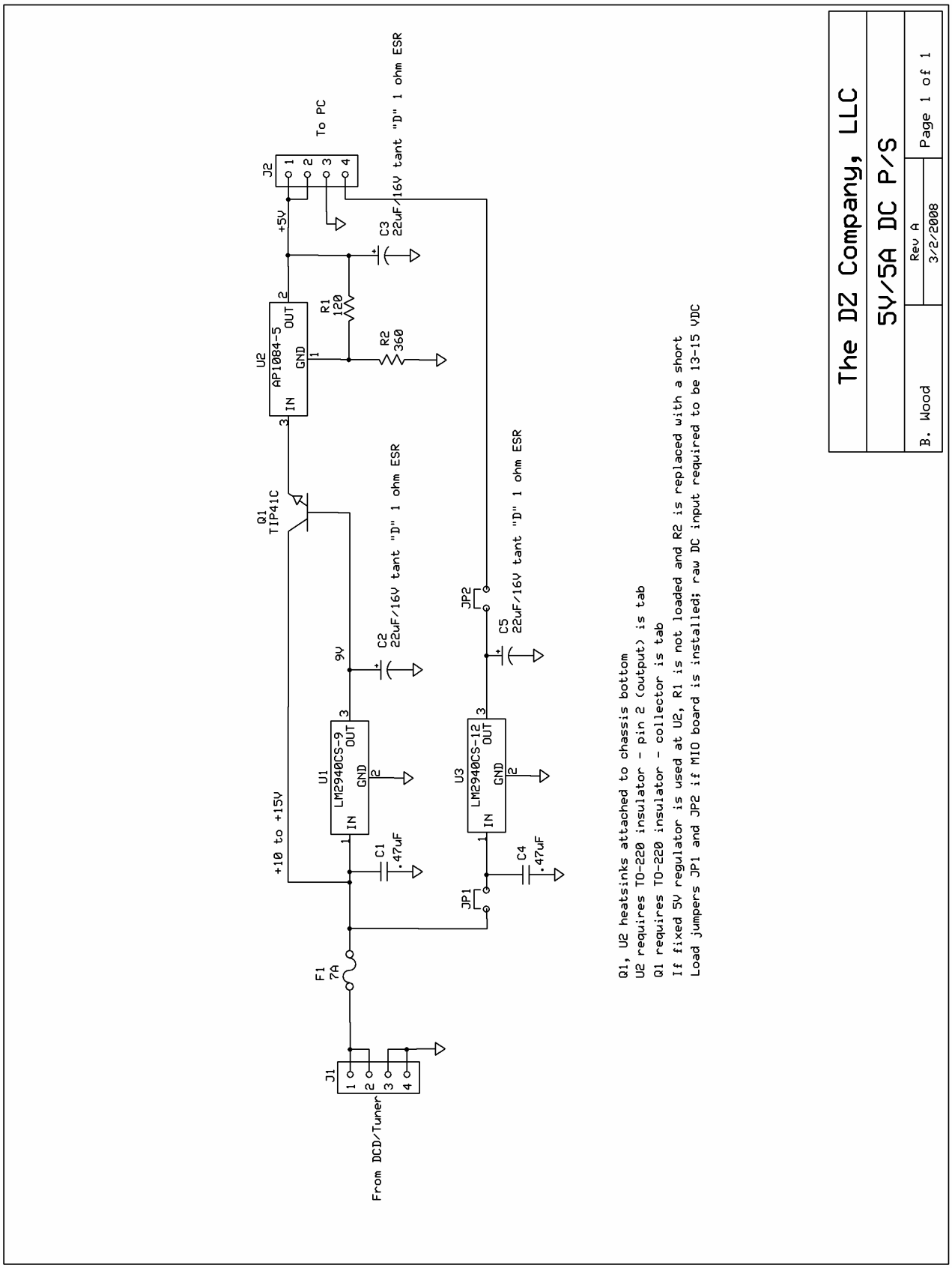
B. Wood
IF Amplifier (455KHz)
AGC derived section
IF derived section
Audio derived section
Buffer
Notch filter/DSP
3.75-5.75V
2.35V-3.75V nom
0-2V
0-.1V
MC1350
TL072
LM358
MMBT3904
MMBF3201
TN2106
1N5711
S-meter
IFAmp
AGC Ampl
AGCSlow
AGCOff
AGCOD
SDA
SCL
VCC
-9V
-5V
RFG
AGC
GADJ
XFO1
TP1
T36-1
T1
L5
120uH var

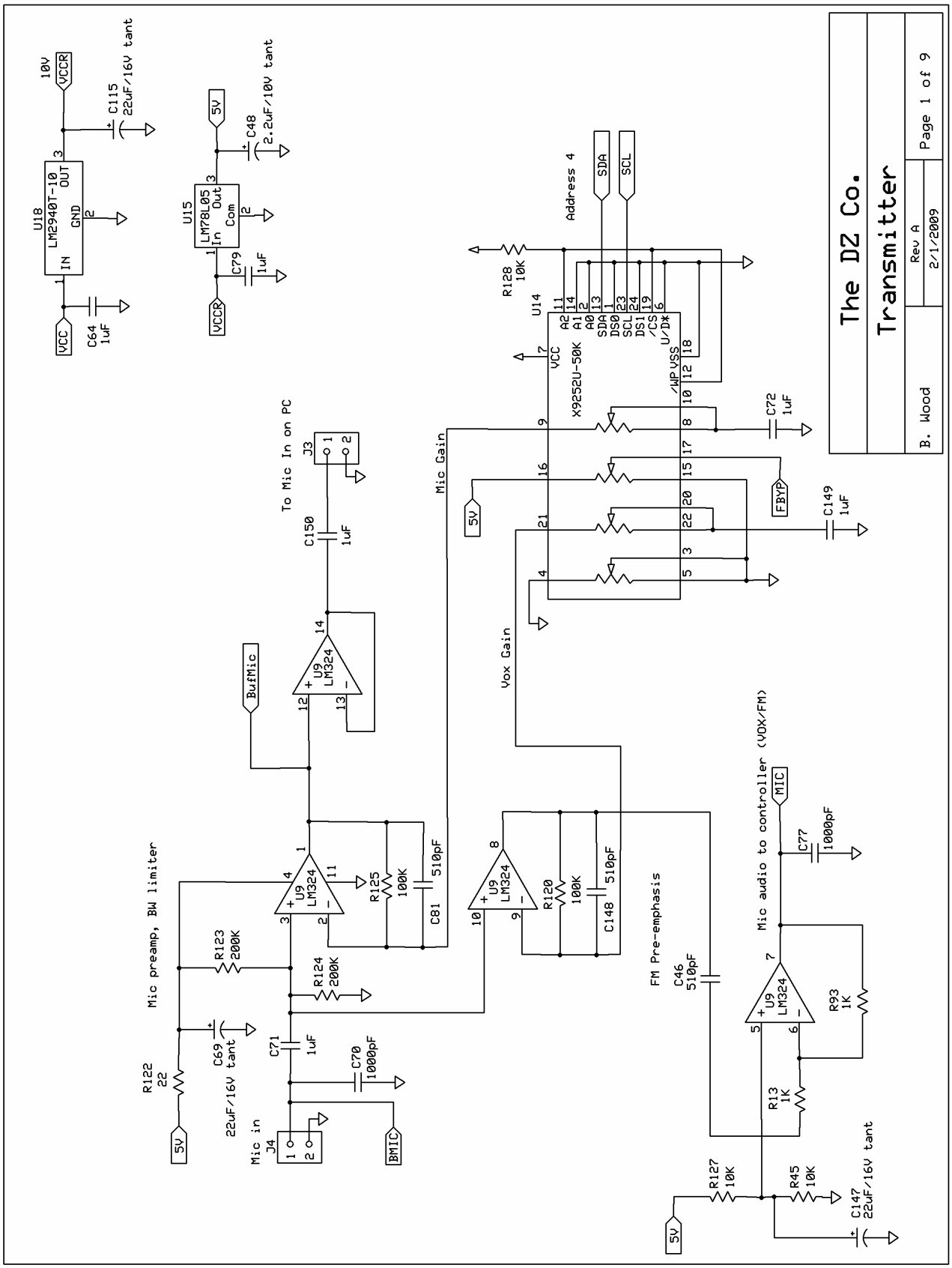

The DZ Co.
Receiver
B. Wood
Rev A
7/12/2008
Page 7 of 9
Detectors
AM Detector
Product Detector
BFOA (455 KHz)
455KHz/20KHz
S-meter
Meter
Tx Meter
RSSI
TxMeter
AM
AGC Ampl
CWSB
VCC
5V
XFO1
ModeAM
/ModeFM
/MtrRx
/MtrTx
U26 AD8000
U7 SA612
U28 LM358
U21 CD4066
FL2 LTM455DU
Q24 TN2106
Q25 TN2106
Q26 TN2106
Q28 TN2106
Q29 TN2106
Q18 TN2106
D6 1N5711
D15 1N5711
D16 1N914
D17 1N914
D19 1N914
D20 1N914
C2 1uF
C16 1uF
C151 22uF/16V tant
C83 .1uF
C85 .1uF
C72 .1uF
C159 .1uF
C33 .1uF
C154 .1uF
C152 .1uF
C156 .1uF
C23 1uF
C6 .015uF
C153 .015uF
C15 1000pF
C176 10pF
C177 10pF
R22 10K
R122 10
R120 470
R121 47
R158 3.9K
R39 3.9K
R172 10
R23 470
R32 470
R97 470
R93 10K
R134 1K
R133 1K
R132 1K
R149 20K
R160 20K
R99 47
RV2 100K
RFC1 1mH
RFC2 1mH
RFC3 1mH
RFC4 1mH
LO4 250mVp-p
J1
J19 Meter
J25 Tx Meter

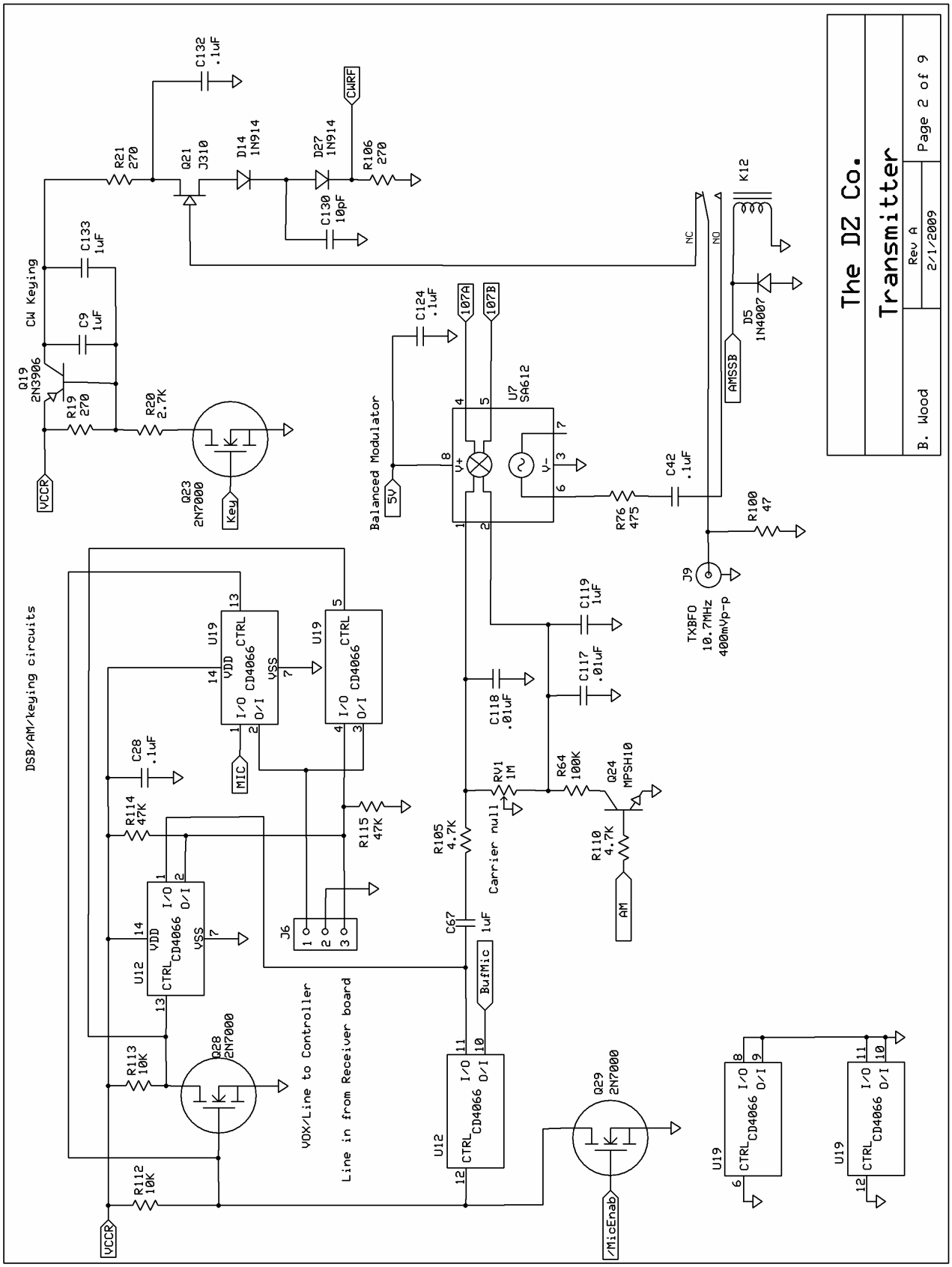

The DZ Co.
Receiver
Rev A
7/12/2008
Page 8 of 9
B. Wood
U15 X9460 33K pots
U23 DAC5573
U4 TL072
U14 LM79L05
U13 LM78L05
Q27 TN2106
Q32 TN2106
Q31 TN2106
Q34 MMBF5460
1N5711 D2
Adr=2
Adr=3
FullDup
Line Out to PC's Line In
nom S9 = 200mVrms
Ext Out to rear panel
(and NBThr)
VCC
-9V
-5V
5V
SDA
SCL
AM
CWSB
FM
APWR
LPTT
GADJ
VR
VL
TxMeter
RFG
FM Sql

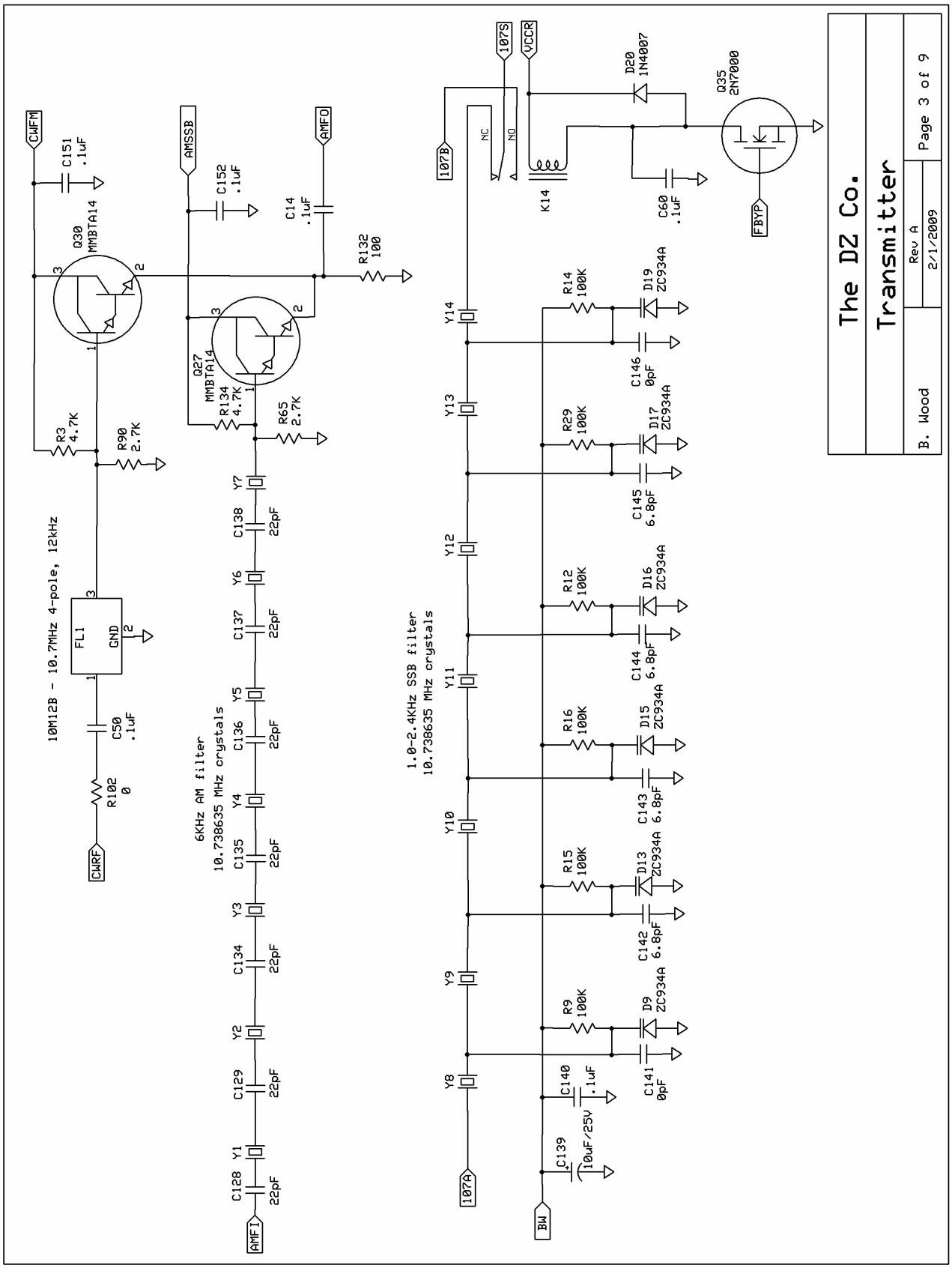

The DZ Co.
Receiver
Rev A
7/12/2008
Page 9 of 9
B. Wood
Antivox buffer
Heatsink
Pins 3,4,5,10,11,12
Line In from PC
Line out
To Tx
Ext In from rear panel
Sidetone
MutePC
SPKRR+
SPKRR-
SPKRL+
SPKRL-
HPR
GND
HPL
VOX
AVOX
APWR
VR
VL
SCL
SDA
LM380
LM348
X9460
33K pots
CD4066
5V
-5V


The DZ Company, LLC
RS232C interconnect
B. Wood
Rev A
5/13/2008
Page 1 of 1
J2
J1
RXD
RTS
TXD
CTS
DTR
GND
R1 100
R2 100
R3 100
R4 100
R5 100
C1 .01uF
C2 .01uF
C3 .01uF
C4 .01uF
C5 .01uF


The DZ Company, LLC
5V/5A DC P/S
B. Wood
Rev A
3/2/2008
Page 1 of 1
J1
From DCD/Tuner
F1
7A
+10 to +15V
U1
LM2940CS-9
IN
OUT
GND
C1
.47uF
9V
C2
22uF/16V tant "D" 1 ohm ESR
U3
LM2940CS-12
C4
.47uF
JP1
JP2
C5
22uF/16V tant "D" 1 ohm ESR
Q1
TIP41C
U2
AP1084-5
R1
120
R2
360
+5V
C3
22uF/16V tant "D" 1 ohm ESR
J2
To PC
Q1, U2 heatsinks attached to chassis bottom
U2 requires TO-220 insulator - pin 2 (output) is tab
Q1 requires TO-220 insulator - collector is tab
If fixed 5V regulator is used at U2, R1 is not loaded and R2 is replaced with a short
Load jumpers JP1 and JP2 if MIO board is installed; raw DC input required to be 13-15 VDC


The DZ Co.
Transmitter
B. Wood
Rev A
2/1/2009
Page 1 of 9
U18
LM2940T-10
IN
GND
OUT
10V
VCCR
C115
22uF/16V tant
C64
1uF
VCC
U15
LM78L05
In
Out
Com
5V
C48
2.2uF/10V tant
C79
1uF
VCCR
R128
10K
Address 4
SDA
SCL
U14
X9252U-50K
A2
A1
A0
SDA
DS0
SCL
DS1
/CS
U/D
/WP
VSS
VCC
C72
1uF
FBYP
C149
1uF
Mic Gain
Vox Gain
To Mic In on PC
J3
C150
1uF
U9
LM324
BufMic
Mic preamp, BW limiter
R123
200K
R124
200K
R125
100K
C81
510pF
R120
100K
C148
510pF
FM Pre-emphasis
C46
510pF
Mic audio to controller (VOX/FM)
MIC
C77
1000pF
R93
1K
R13
1K
R127
10K
R45
10K
C147
22uF/16V tant
R122
22
C69
22uF/16V tant
C71
1uF
C70
1000pF
Mic in
J4
BMIC


The DZ Co.
Transmitter
Rev A
2/1/2009
B. Wood
Page 2 of 9
DSB/AM/keying circuits
CW Keying
Balanced Modulator
Carrier null
VOX/Line to Controller
Line in from Receiver board
TXBFO
10.7MHz
400mVp-p
Q19 2N3906
R19 270
R20 2.7K
Q23 2N7000
Key
C9 1uF
C133 1uF
C132 .1uF
R21 270
Q21 J310
D14 1N914
D27 1N914
CWRF
R106 270
C130 10pF
K12
NC
NO
D5 1N4007
AMSSB
C124 .1uF
107A
107B
U7 SA612
5V
C42 .1uF
R76 475
R100 47
J9
C119 1uF
C117 .01uF
C118 .01uF
U19 CD4066
MIC
C28 .1uF
R114 47K
R115 47K
U12 CD4066
R105 4.7K
RV1 1M
R64 100K
Q24 MPSH10
R110 4.7K
AM
C67 1uF
BufMic
J6
Q28 2N7000
R113 10K
R112 10K
Q29 2N7000
/MicEnab
VCCR


The DZ Co.
Transmitter
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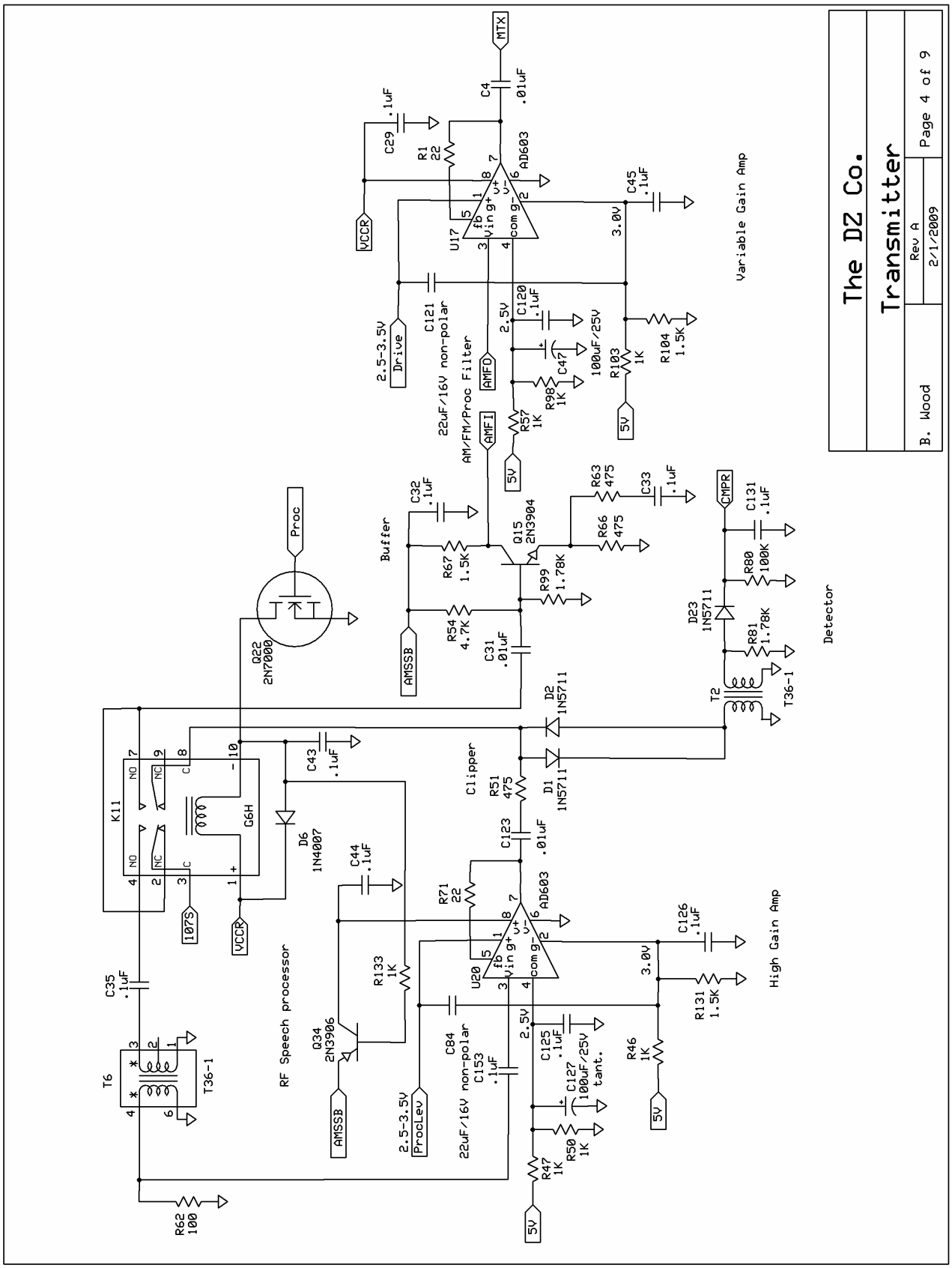
CWFM
CWRF
AMSSB
AMFD
AMFI
C151 .1uF
C152 .1uF
C14 .1uF
C50 .1uF
C60 .1uF
C139 10uF/25V
C140 .1uF
C141 0pF
C142 6.8pF
C143 6.8pF
C144 6.8pF
C145 6.8pF
C146 0pF
Q30 MMBTA14
Q27 MMBTA14
Q35 2N7000
R3 4.7K
R90 2.7K
R134 4.7K
R65 2.7K
R132 100
R102 0
R9 100K
R12 100K
R14 100K
R15 100K
R16 100K
R29 100K
D9 ZC934A
D13 ZC934A
D15 ZC934A
D16 ZC934A
D17 ZC934A
D19 ZC934A
D20 1N4007
FL1
GND
10M12B - 10.7MHz 4-pole, 12kHz
6KHz AM filter
10.738635 MHz crystals
1.0-2.4KHz SSB filter
10.738635 MHz crystals
C128 22pF
C129 22pF
C134 22pF
C135 22pF
C136 22pF
C137 22pF
C138 22pF
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
Y10
Y11
Y12
Y13
Y14
107A
107B
107S
VCCR
BW
FBYP
K14
NC
NO


The DZ Co.
Transmitter
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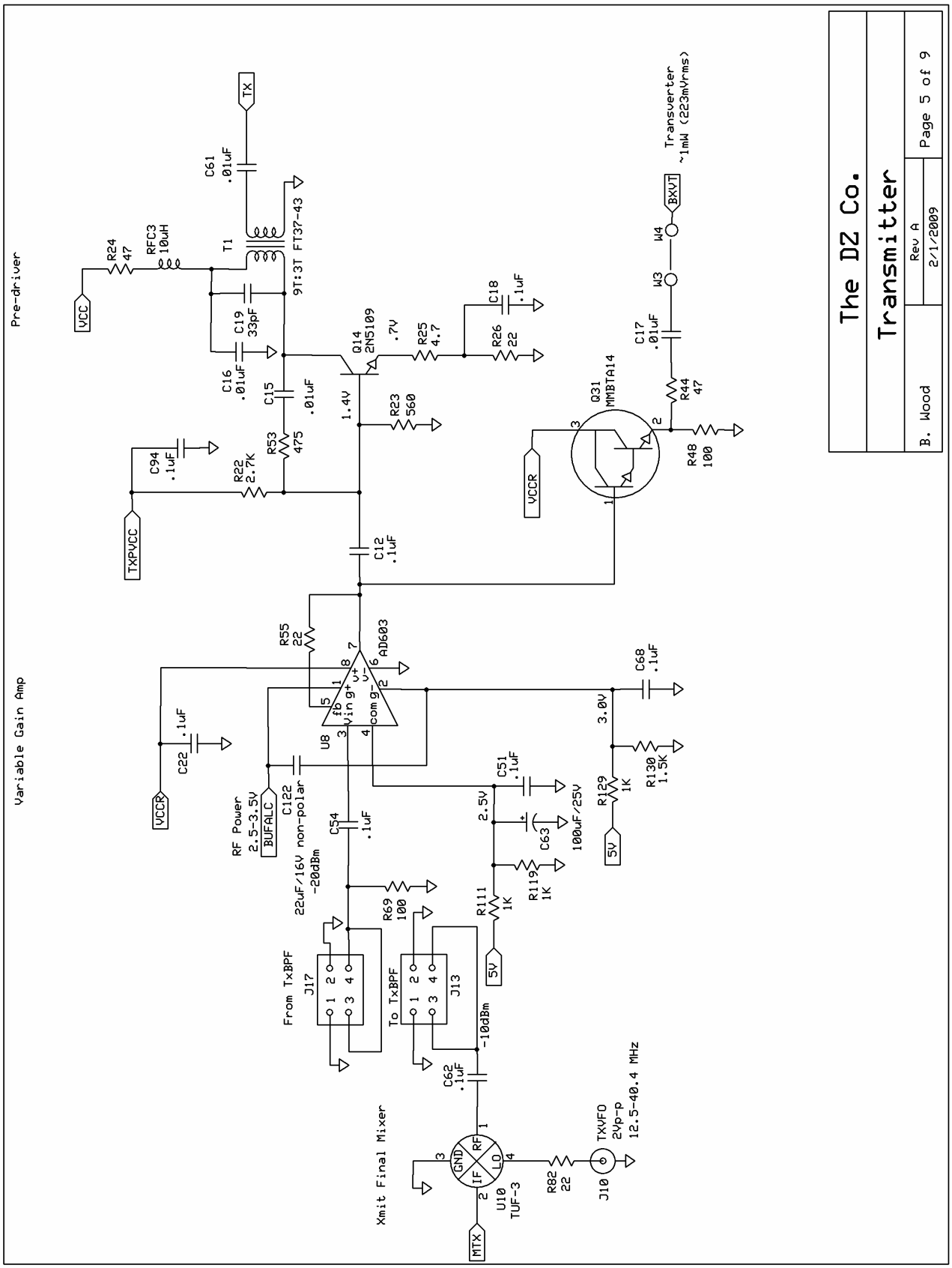
MTX
C4 .01uF
C29 .1uF
R1 22
VCCR
U17 AD603
C45 .1uF
3.0V
Variable Gain Amp
C121 22uF/16V non-polar
2.5-3.5V Drive
AM/FM/Proc Filter
AMFO
2.5V
C120 .1uF
C47 100uF/25V
R103 1K
R104 1.5K
R98 1K
R57 1K
AMFI
5V
Buffer
C32 .1uF
R67 1.5K
Q15 2N3904
R63 475
R66 475
C33 .1uF
CMPR
C131 .1uF
R80 100K
D23 1N5711
R81 1.78K
T2
T36-1
Detector
Proc
Q22 2N7000
AMSSB
R54 4.7K
C31 .01uF
R99 1.78K
D2 1N5711
C43 .1uF
Clipper
R51 475
D1 1N5711
K11
G6H
D6 1N4007
C44 .1uF
C123 .01uF
R71 22
U20 AD603
C126 .1uF
R131 1.5K
High Gain Amp
107S
VCCR
C35 .1uF
T6
T36-1
RF Speech processor
R133 1K
Q34 2N3906
C84 non-polar
C153 .1uF
2.5-3.5V ProcLev
22uF/16V
C125 .1uF
C127 100uF/25V tant.
R46 1K
R50 1K
R47 1K
R62 100


The DZ Co.
Transmitter
B. Wood
Rev A
2/1/2009
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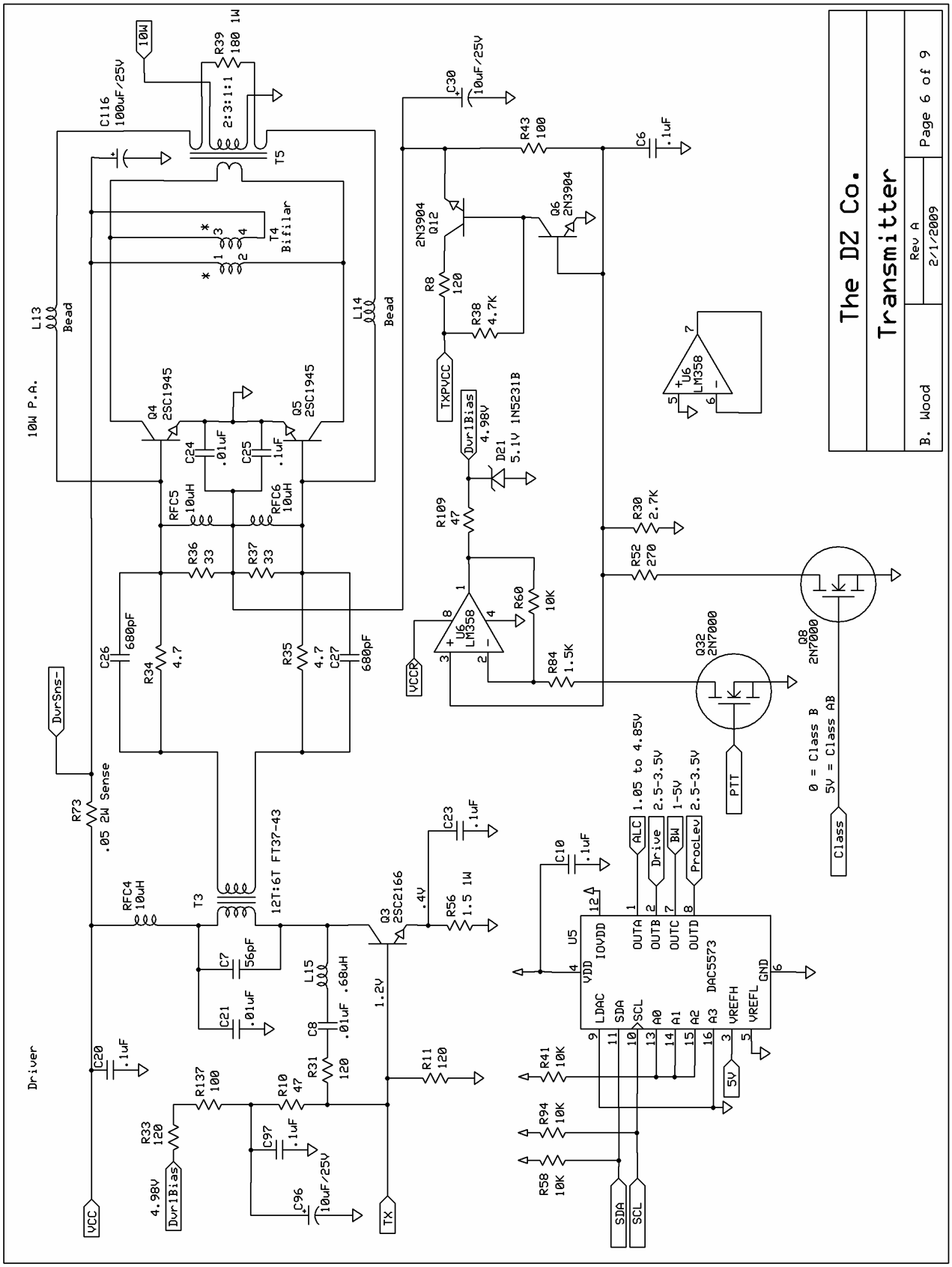
Pre-driver
Variable Gain Amp
Xmit Final Mixer
Transverter
~1mW (223mVrms)
9T:3T FT37-43
AD603
TUF-3
2N5109
MMBTA14
From TxBPF
To TxBPF
RF Power
2.5-3.5V
22uF/16V non-polar
-20dBm
-10dBm
100uF/25V
TXVFO
2Vp-p
12.5-40.4 MHz
TX
VCC
TXPVCC
VCCR
BUFALC
MTX
BXVT
5V
2.5V
3.0V
1.4V
.7V


The DZ Co.
Transmitter
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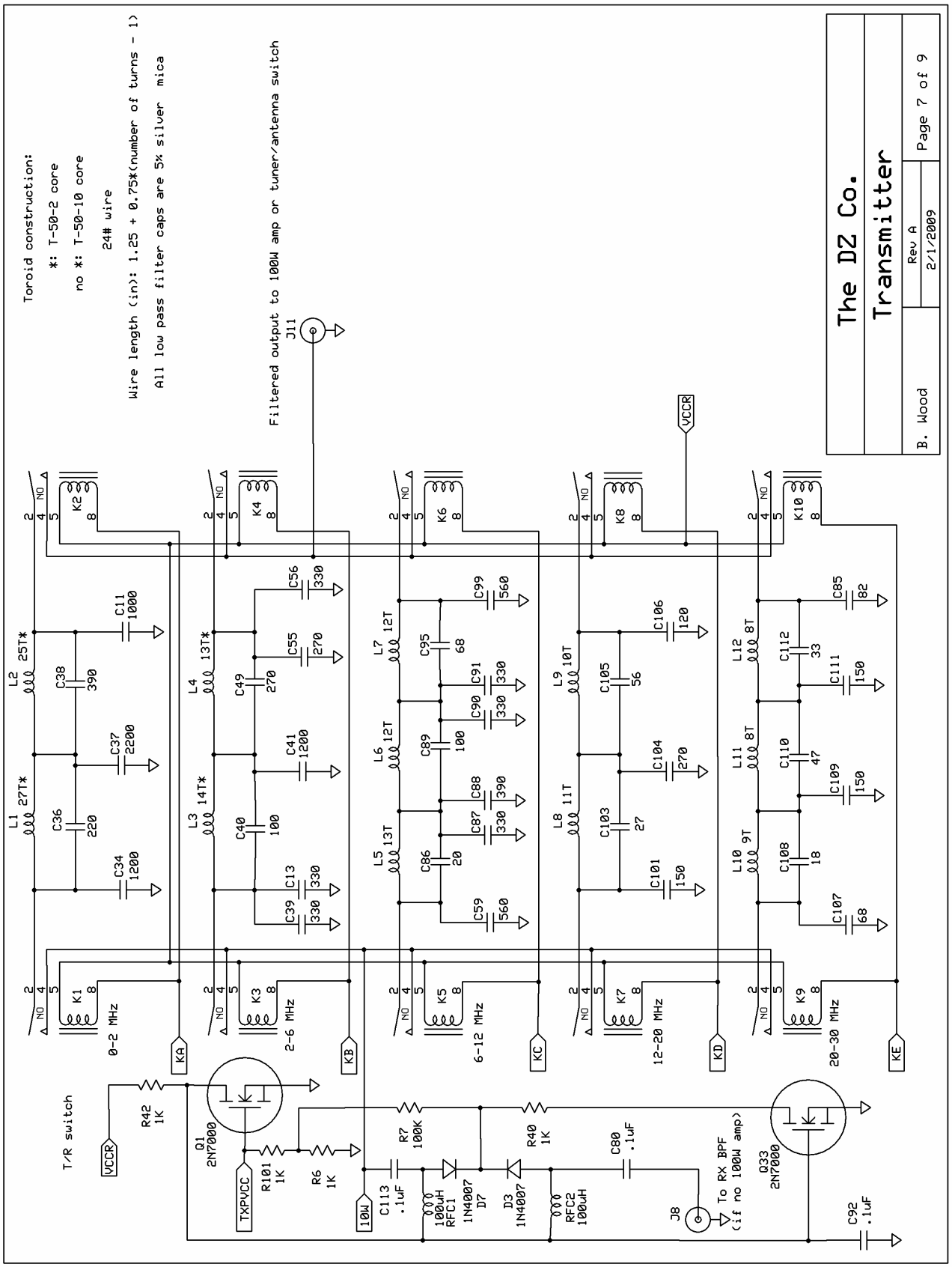
10W P.A.
Driver
DvrSns-
VCC
4.98V
DvrIBias
TX
SDA
SCL
TXPVCC
VCCR
PTT
Class
0 = Class B
5V = Class AB
1.05 to 4.85V
2.5-3.5V
1-5V
2.5-3.5V
ALC
Drive
BW
ProcLev
5V
10W
2:3:1:1
T5
T4
Bifilar
T3
12T:6T FT37-43
L13
L14
Bead
RFC4 10uH
RFC5 10uH
RFC6 10uH
L15 .68uH
R73 .05 2W Sense
R34 4.7
R35 4.7
R36 33
R37 33
R137 100
R33 120
R10 47
R31 120
R11 120
R56 1.5 1W
R8 120
R38 4.7K
R109 47
R60 10K
R84 1.5K
R52 270
R30 2.7K
R43 100
R41 10K
R94 10K
R58 10K
C116 100uF/25V
C30 10uF/25V
C96 10uF/25V
C97 .1uF
C20 .1uF
C21 .01uF
C7 56pF
C8 .01uF
C10 .1uF
C23 .1uF
C24 .01uF
C25 .1uF
C26 680pF
C27 680pF
C6 .1uF
Q4 2SC1945
Q5 2SC1945
Q3 2SC2166
Q12 2N3904
Q6 2N3904
Q32 2N7000
Q8 2N7000
D21 5.1V 1N5231B
U6 LM358
U5 DAC5573
IOVDD
VDD
LDAC
SDA
SCL
A0
A1
A2
A3
VREFH
VREFL
GND
OUTA
OUTB
OUTC
OUTD


Toroid construction:
*: T-50-2 core
no *: T-50-10 core
24# wire
Wire length (in): 1.25 + 0.75*(number of turns - 1)
All low pass filter caps are 5% silver mica
Filtered output to 100W amp or tuner/antenna switch
J11
The DZ Co.
Transmitter
B. Wood
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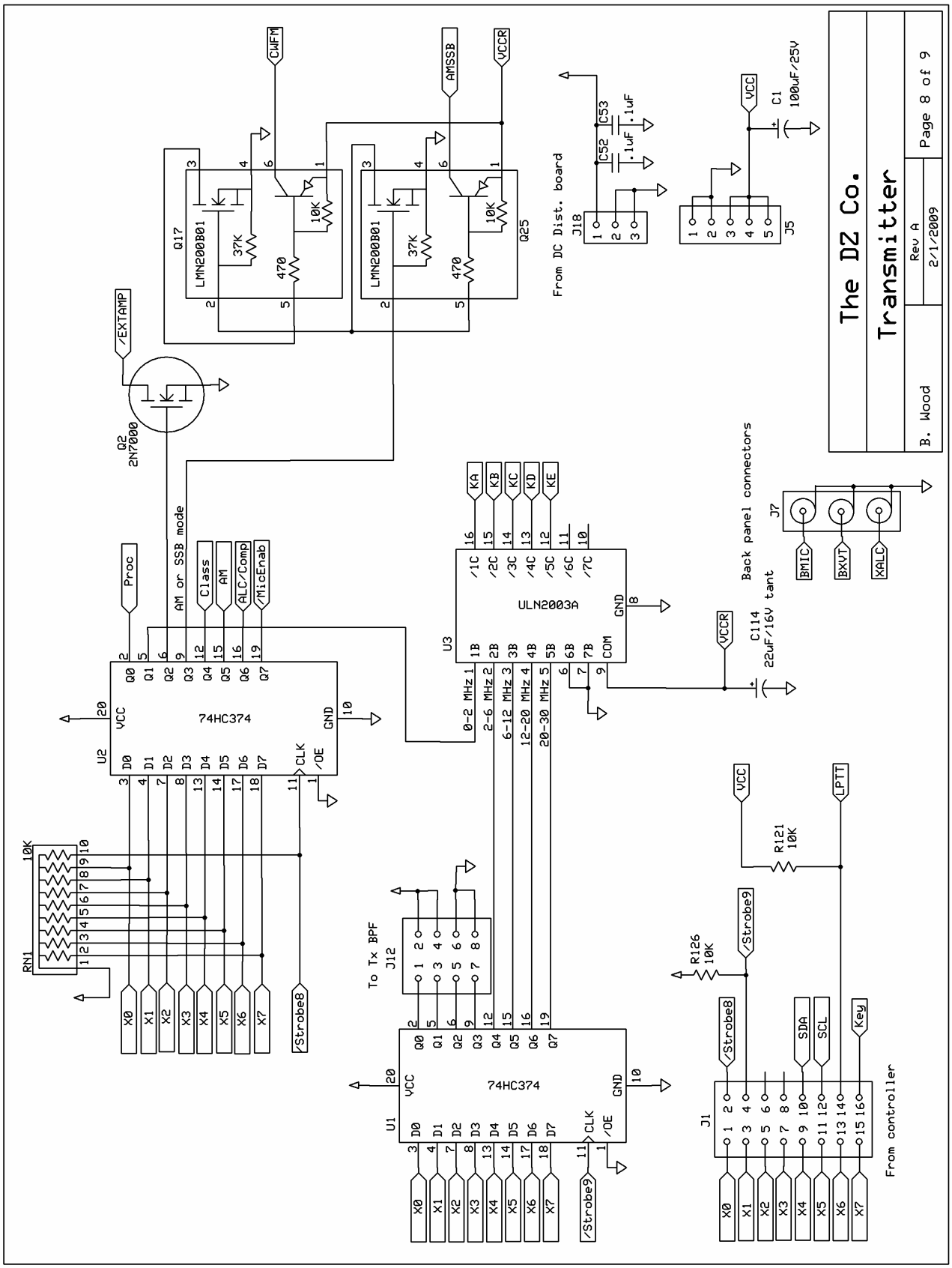
VCCR
T/R switch
R42 1K
Q1 2N7000
R101 1K
R6 1K
R7 100K
R40 1K
C80 .1uF
C113 .1uF
C92 .1uF
TXPVCC
10W
RFC1 100uH
D7 1N4007
D3 1N4007
RFC2 100uH
J8
To RX BPF (if no 100W amp)
Q33 2N7000
K1
K2
K3
K4
K5
K6
K7
K8
K9
K10
0-2 MHz
2-6 MHz
6-12 MHz
12-20 MHz
20-30 MHz
KA
KB
KC
KD
KE
L1 27T*
L2 25T*
L3 14T*
L4 13T*
L5 13T
L6 12T
L7 12T
L8 11T
L9 10T
L10 9T
L11 8T
L12 8T
C34 1200
C36 220
C37 2200
C38 390
C11 1000
C39 330
C40 100
C41 1200
C49 270
C13 330
C55 270
C56 330
C59 560
C86 20
C87 330
C88 390
C89 100
C90 330
C91 330
C95 68
C99 560
C101 150
C103 27
C104 270
C105 56
C106 120
C107 68
C108 18
C109 150
C110 47
C111 150
C112 33
C85 82


The DZ Co.
Transmitter
B. Wood
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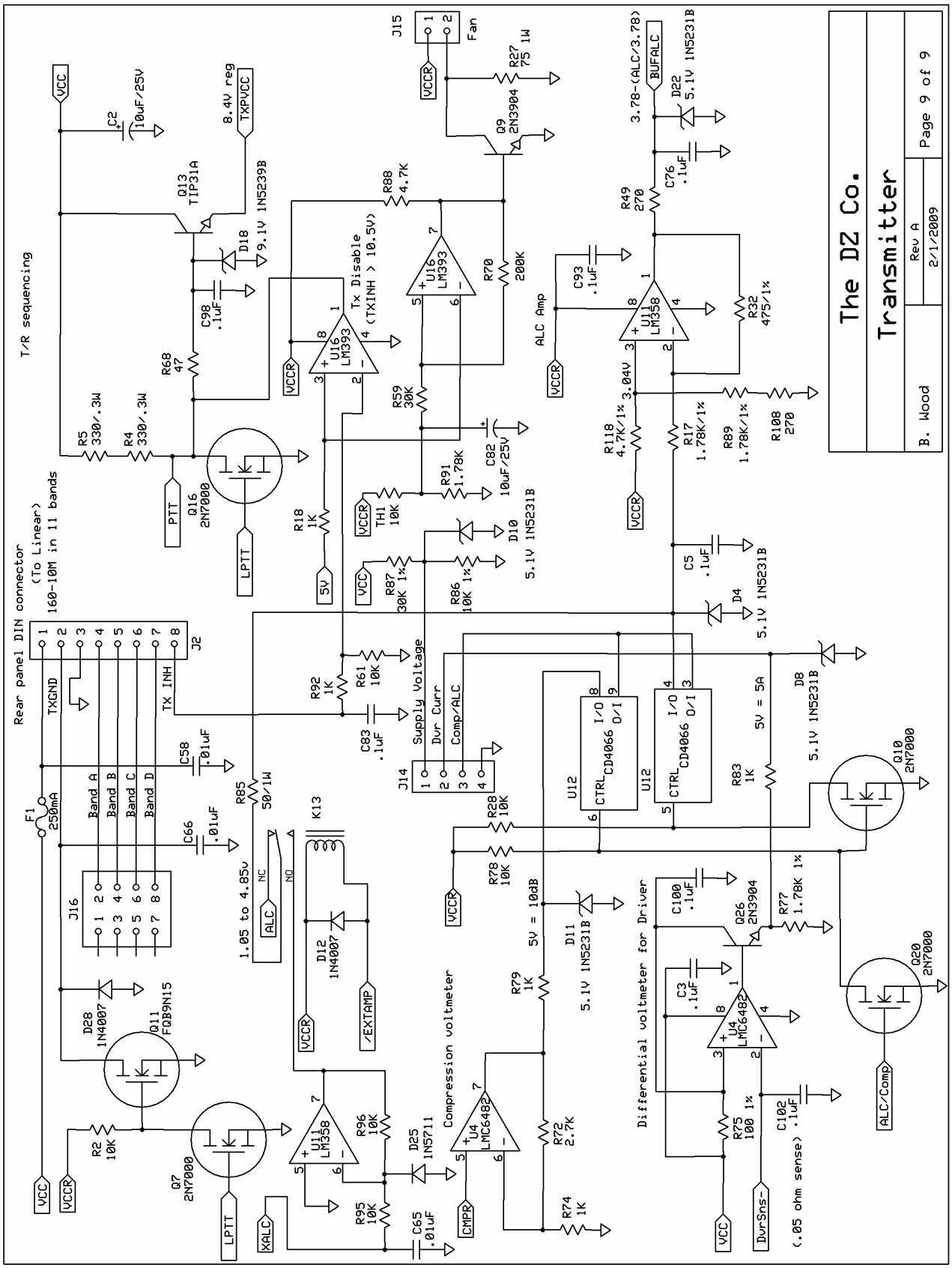
Q17
LMN200B01
Q25
LMN200B01
37K
470
10K
CWFM
AMSSB
VCCR
/EXTAMP
Q2
2N7000
From DC Dist. board
J18
C52
C53
.1uF
.1uF
VCC
C1
100uF/25V
J5
AM or SSB mode
Proc
Class
AM
ALC/Comp
/MicEnab
74HC374
U2
VCC
GND
CLK
/OE
D0
D1
D2
D3
D4
D5
D6
D7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
RN1
10K
X0
X1
X2
X3
X4
X5
X6
X7
/Strobe8
U3
ULN2003A
/1C
/2C
/3C
/4C
/5C
/6C
/7C
COM
GND
1B
2B
3B
4B
5B
6B
7B
KA
KB
KC
KD
KE
0-2 MHz
2-6 MHz
6-12 MHz
12-20 MHz
20-30 MHz
VCCR
C114
22uF/16V tant
Back panel connectors
J7
BMIC
BXVT
XALC
To Tx BPF
J12
74HC374
U1
/Strobe9
R126
10K
R121
10K
LPTT
/Strobe8
SDA
SCL
Key
J1
From controller


The DZ Co.
Transmitter
B. Wood
Rev A
2/1/2009
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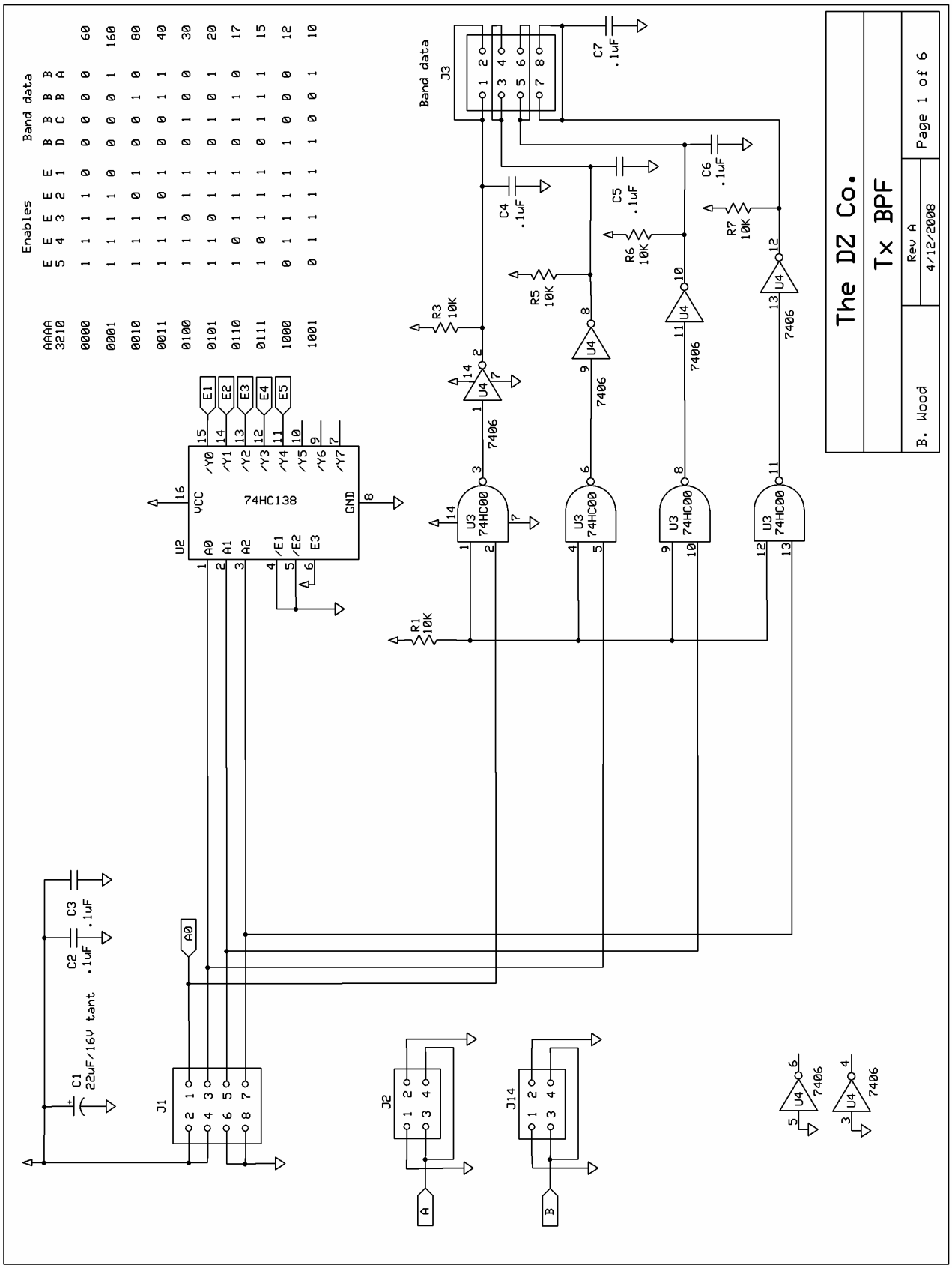
T/R sequencing
Rear panel DIN connector
(To Linear)
160-10M in 11 bands
Tx Disable
(TXINH > 10.5V)
ALC Amp
Supply Voltage
Dvr Curr
Comp/ALC
Compression voltmeter
Differential voltmeter for Driver
1.05 to 4.85v
5V = 10dB
5V = 5A
3.78-(ALC/3.78)
(.05 ohm sense)
Fan
VCC
VCCR
TXPVCC
BUFALC
PTT
LPTT
XALC
CMPR
ALC/Comp
DvrSns-
/EXTAMP
TXGND
TX INH
Band A
Band B
Band C
Band D
8.4V reg
9.1V 1N5239B
5.1V 1N5231B
3.04V
Q13 TIP31A
Q16 2N7000
Q7 2N7000
Q11 FQB9N15
Q9 2N3904
Q26 2N3904
Q10 2N7000
Q20 2N7000
U16 LM393
U11 LM358
U4 LMC6482
U12 CD4066
K13
ALC
NC
NO
J2
J14
J15
J16
F1 250mA
C2 10uF/25V
C98 .1uF
C93 .1uF
C76 .1uF
C58 .01uF
C66 .01uF
C83 .1uF
C5 .1uF
C3 .1uF
C100 .1uF
C102 .1uF
C65 .01uF
C82 10uF/25V
R5 330/.3W
R4 330/.3W
R68 47
R88 4.7K
R70 200K
R59 30K
R91 1.78K
R18 1K
TH1 10K
R87 30K 1%
R86 10K 1%
R92 1K
R61 10K
R85 50/1W
R28 10K
R78 10K
R79 1K
R72 2.7K
R74 1K
R96 10K
R95 10K
R2 10K
R75 100 1%
R77 1.78K 1%
R83 1K
R49 270
R32 475/1%
R118 4.7K/1%
R17 1.78K/1%
R89 1.78K/1%
R108 270
R27 75 1W
D18
D10
D4
D8
D11
D12 1N4007
D28 1N4007
D25 1N5711
D22 5.1V 1N5231B


Enables
Band data
AAAA 3210
E E E E E 5 4 3 2 1
B B B B B D C B A
0000 1 1 1 1 1 0 0 0 0 0 0 60
0001 1 1 1 1 0 0 0 0 0 1 0 160
0010 1 1 1 0 1 0 0 0 1 0 0 80
0011 1 1 1 0 1 0 0 0 1 1 0 40
0100 1 1 0 1 1 0 0 1 0 0 0 30
0101 1 1 0 1 1 0 0 1 0 1 0 20
0110 1 0 1 1 1 0 0 1 1 0 0 17
0111 1 0 1 1 1 0 0 1 1 1 0 15
1000 0 1 1 1 1 1 1 0 0 0 0 12
1001 0 1 1 1 1 1 1 0 0 0 1 10
Band data
J3
C7 .1uF
C6 .1uF
C5 .1uF
C4 .1uF
R7 10K
R6 10K
R5 10K
R3 10K
R1 10K
U4 7406
U3 74HC00
U2 74HC138
VCC
GND
A0
A1
A2
/E1
/E2
E3
/Y0
/Y1
/Y2
/Y3
/Y4
/Y5
/Y6
/Y7
E1
E2
E3
E4
E5
C1 22uF/16V tant
C2 .1uF
C3 .1uF
J1
J2
J14
A
B
The DZ Co.
Tx BPF
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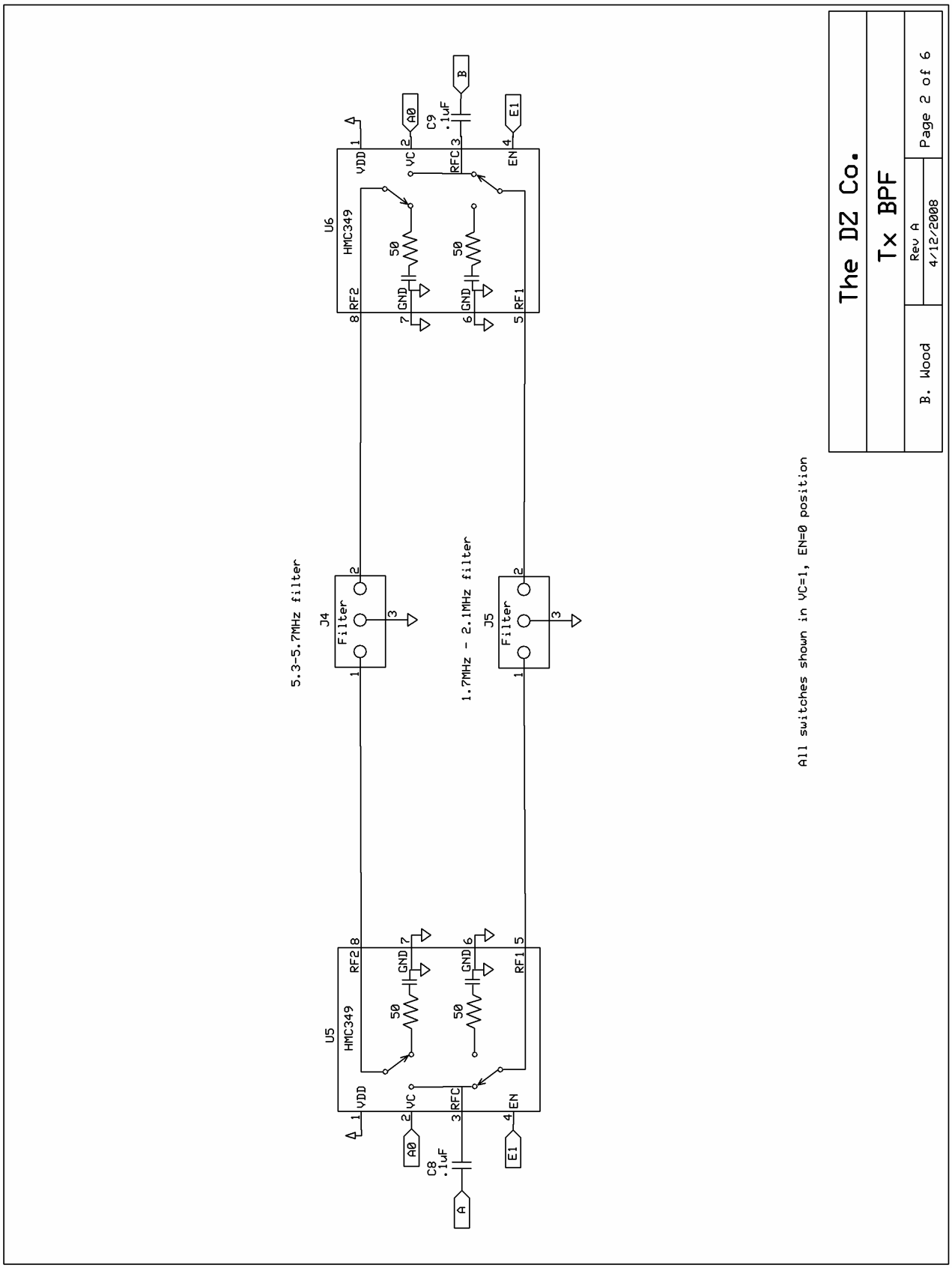
B. Wood


The DZ Co.
Tx BPF
B. Wood
Rev A
4/12/2008
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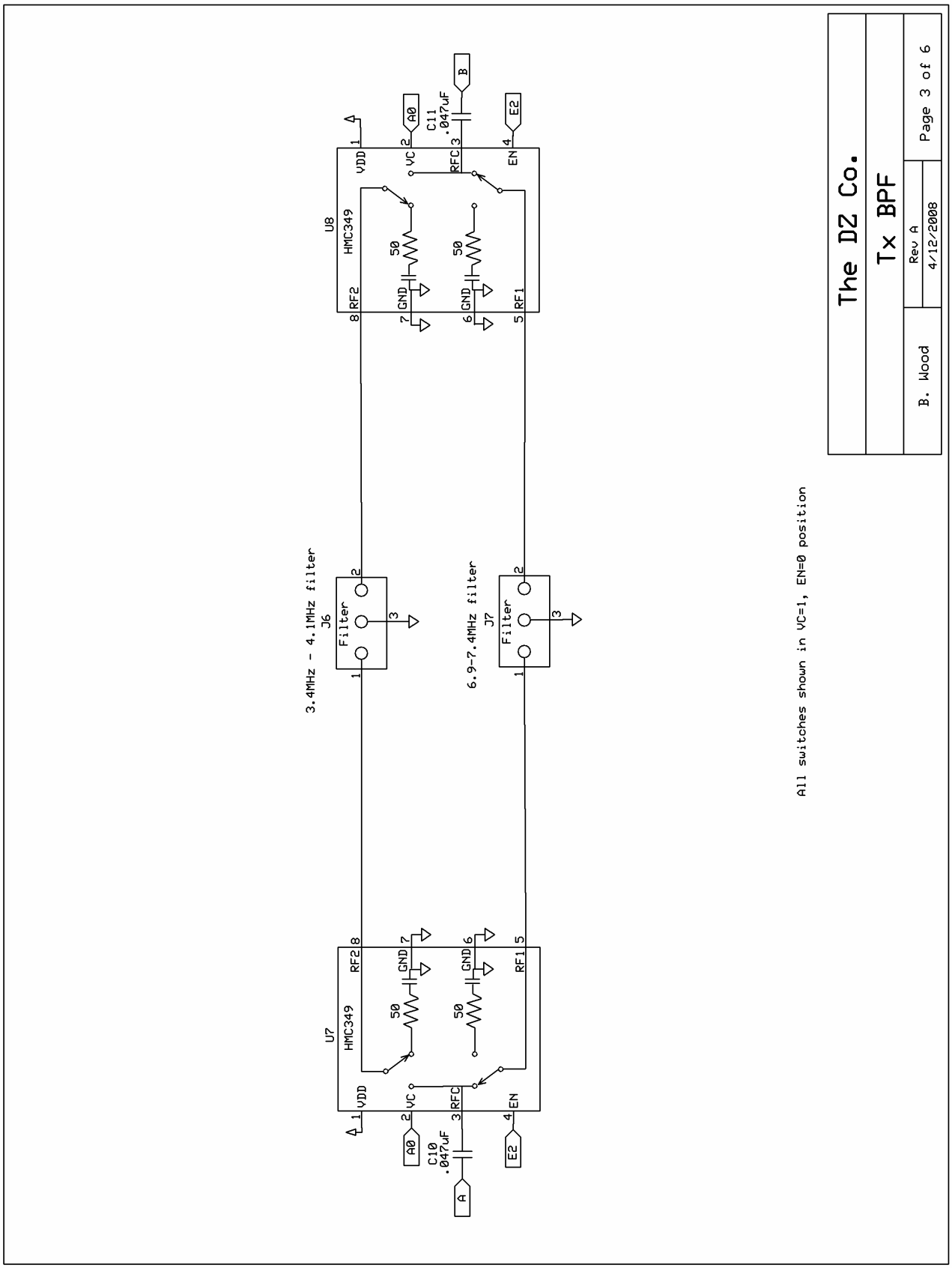
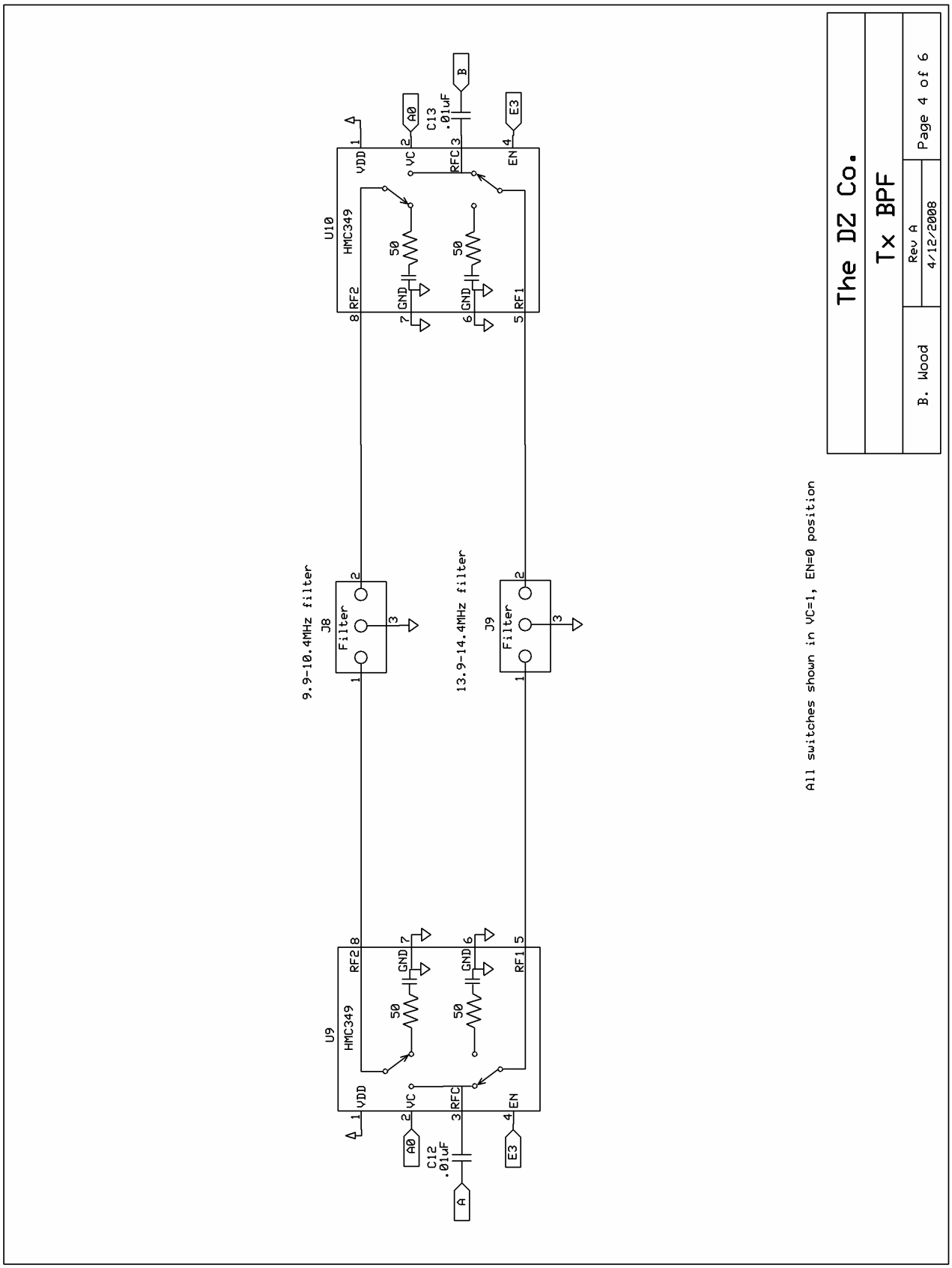
All switches shown in VC=1, EN=0 position
5.3-5.7MHz filter
1.7MHz - 2.1MHz filter
J4
J5
Filter
U5
U6
HMC349
VDD
VC
RFC
EN
RF1
RF2
GND
50
A0
A1
A
B
C8 .1uF
C9 .1uF


The DZ Co.
Tx BPF
B. Wood
Rev A
4/12/2008
Page 3 of 6
All switches shown in VC=1, EN=0 position
3.4MHz - 4.1MHz filter
J6
Filter
6.9-7.4MHz filter
J7
Filter
U7
HMC349
U8
HMC349
VDD
VC
RFC
EN
RF1
RF2
GND
50
A0
A
B
E2
C10
.047uF
C11
.047uF


The DZ Co.
Tx BPF
B. Wood
Rev A
4/12/2008
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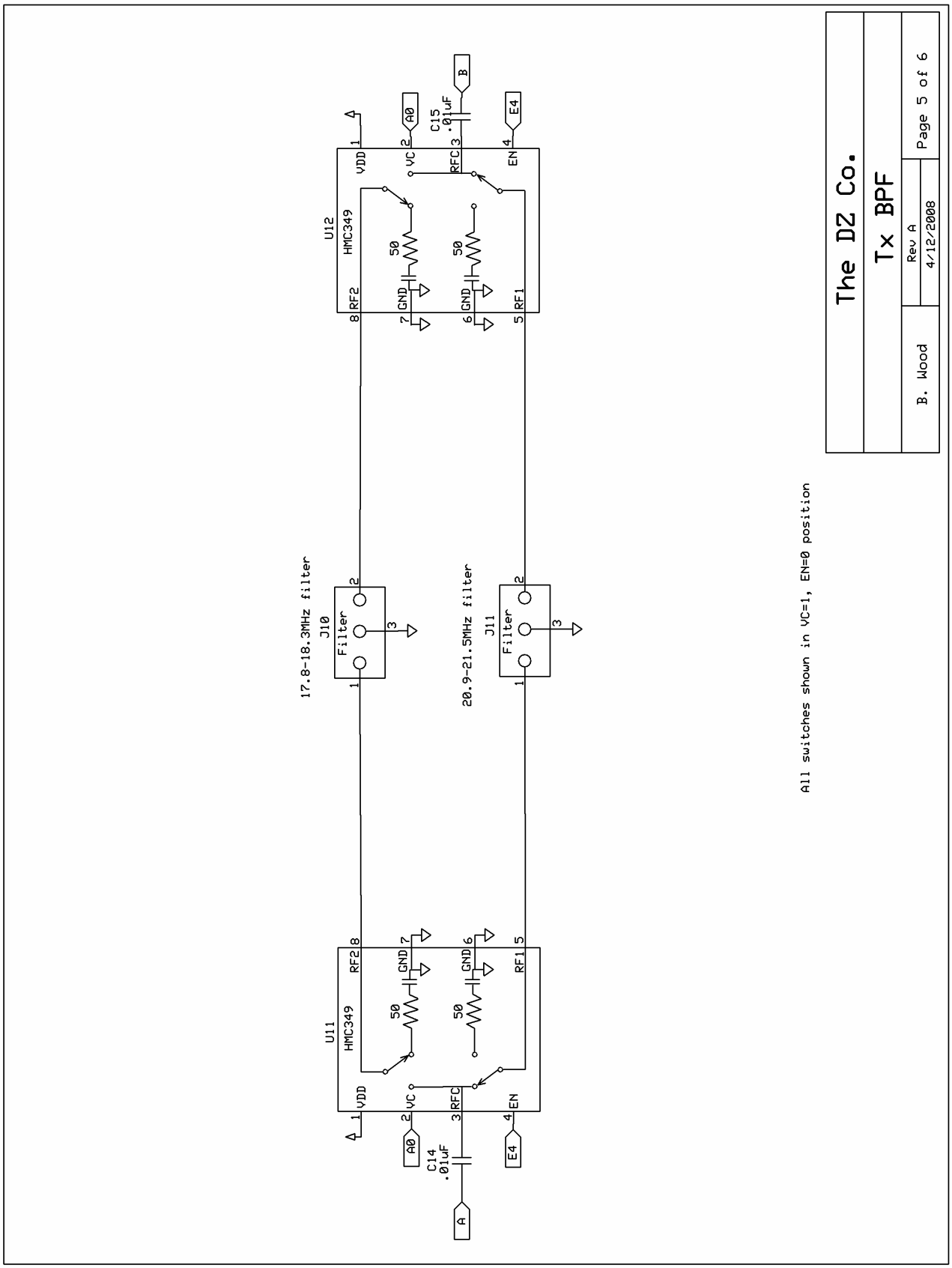
All switches shown in VC=1, EN=0 position
9.9-10.4MHz filter
13.9-14.4MHz filter
J8
J9
Filter
U9
U10
HMC349
VDD
VC
RFC
EN
RF1
RF2
GND
50
A0
E3
A
B
C12
.01uF
C13
.01uF


The DZ Co.
Tx BPF
B. Wood
Rev A
4/12/2008
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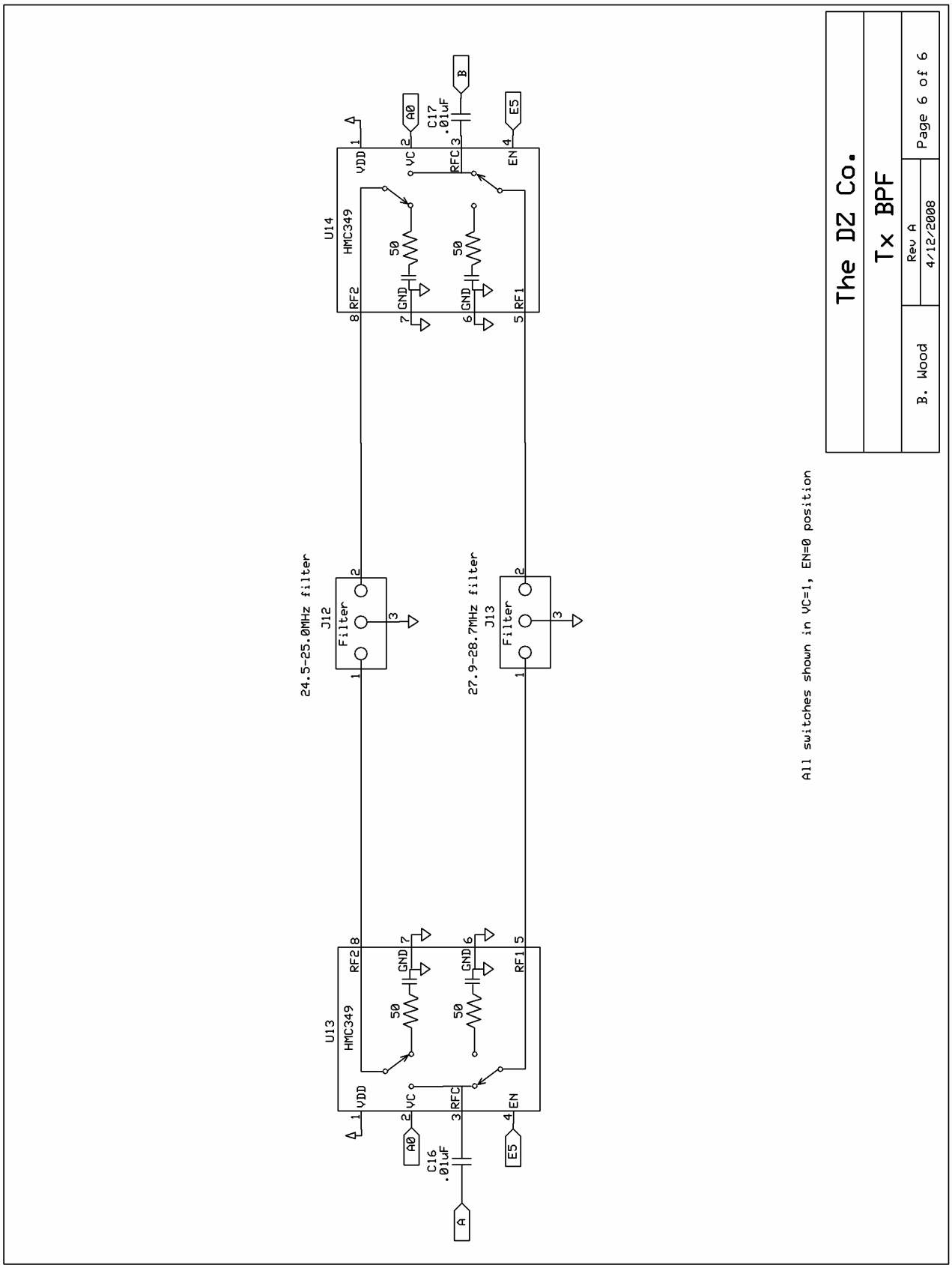
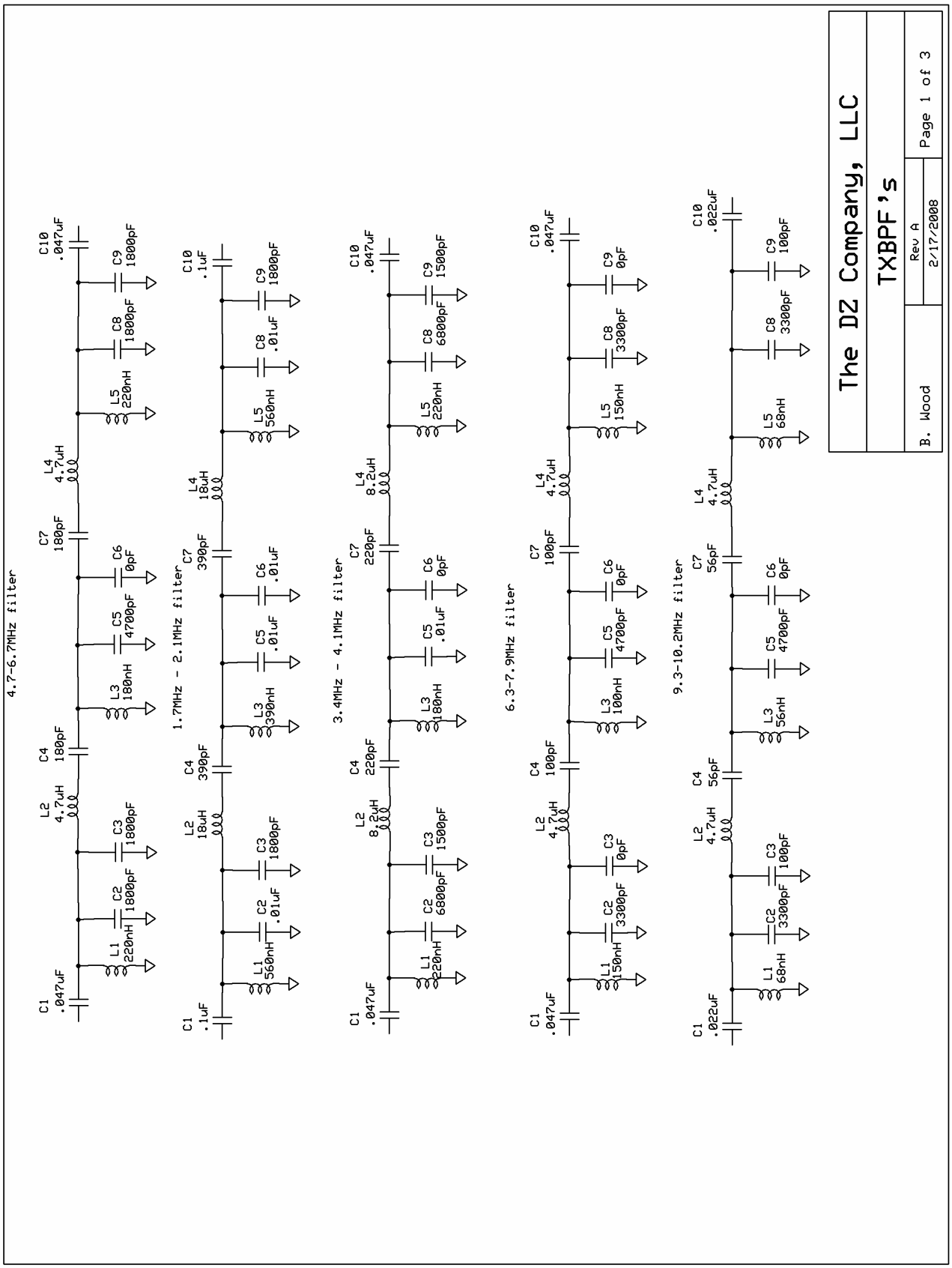
All switches shown in VC=1, EN=0 position
17.8-18.3MHz filter
20.9-21.5MHz filter
J10
J11
Filter
U11
U12
HMC349
VDD
VC
RFC
EN
RF1
RF2
GND
50
A0
E4
A
B
C14
.01uF
C15
.01uF


The DZ Co.
Tx BPF
B. Wood
Rev A
4/12/2008
Page 6 of 6
All switches shown in VC=1, EN=0 position
24.5-25.0MHz filter
27.9-28.7MHz filter
J12
J13
Filter
U13
U14
HMC349
VDD
VC
RFC
EN
RF1
RF2
GND
50
A0
E5
A
B
C16
C17
.01uF


4.7-6.7MHz filter
C1 .047uF
L1 220nH
C2 1800pF
L2 4.7uH
C3 1800pF
C4 180pF
L3 180nH
C5 4700pF
C7 180pF
C6 0pF
L4 4.7uH
L5 220nH
C8 1800pF
C10 .047uF
C9 1800pF
1.7MHz - 2.1MHz filter
C1 .1uF
L1 560nH
C2 .01uF
L2 18uH
C3 1800pF
C4 390pF
L3 390nH
C5 .01uF
C7 390pF
C6 .01uF
L4 18uH
L5 560nH
C8 .01uF
C10 .1uF
C9 1800pF
3.4MHz - 4.1MHz filter
C1 .047uF
L1 220nH
C2 6800pF
L2 8.2uH
C3 1500pF
C4 220pF
L3 180nH
C5 .01uF
C7 220pF
C6 0pF
L4 8.2uH
L5 220nH
C8 6800pF
C10 .047uF
C9 1500pF
6.3-7.9MHz filter
C1 .047uF
L1 150nH
C2 3300pF
L2 4.7uH
C3 0pF
C4 100pF
L3 100nH
C5 4700pF
C7 100pF
C6 0pF
L4 4.7uH
L5 150nH
C8 3300pF
C10 .047uF
C9 0pF
9.3-10.2MHz filter
C1 .022uF
L1 68nH
C2 3300pF
L2 4.7uH
C3 100pF
C4 56pF
L3 56nH
C5 4700pF
C7 56pF
C6 0pF
L4 4.7uH
L5 68nH
C8 3300pF
C10 .022uF
C9 100pF
The DZ Company, LLC
TXBPF's
B. Wood
Rev A
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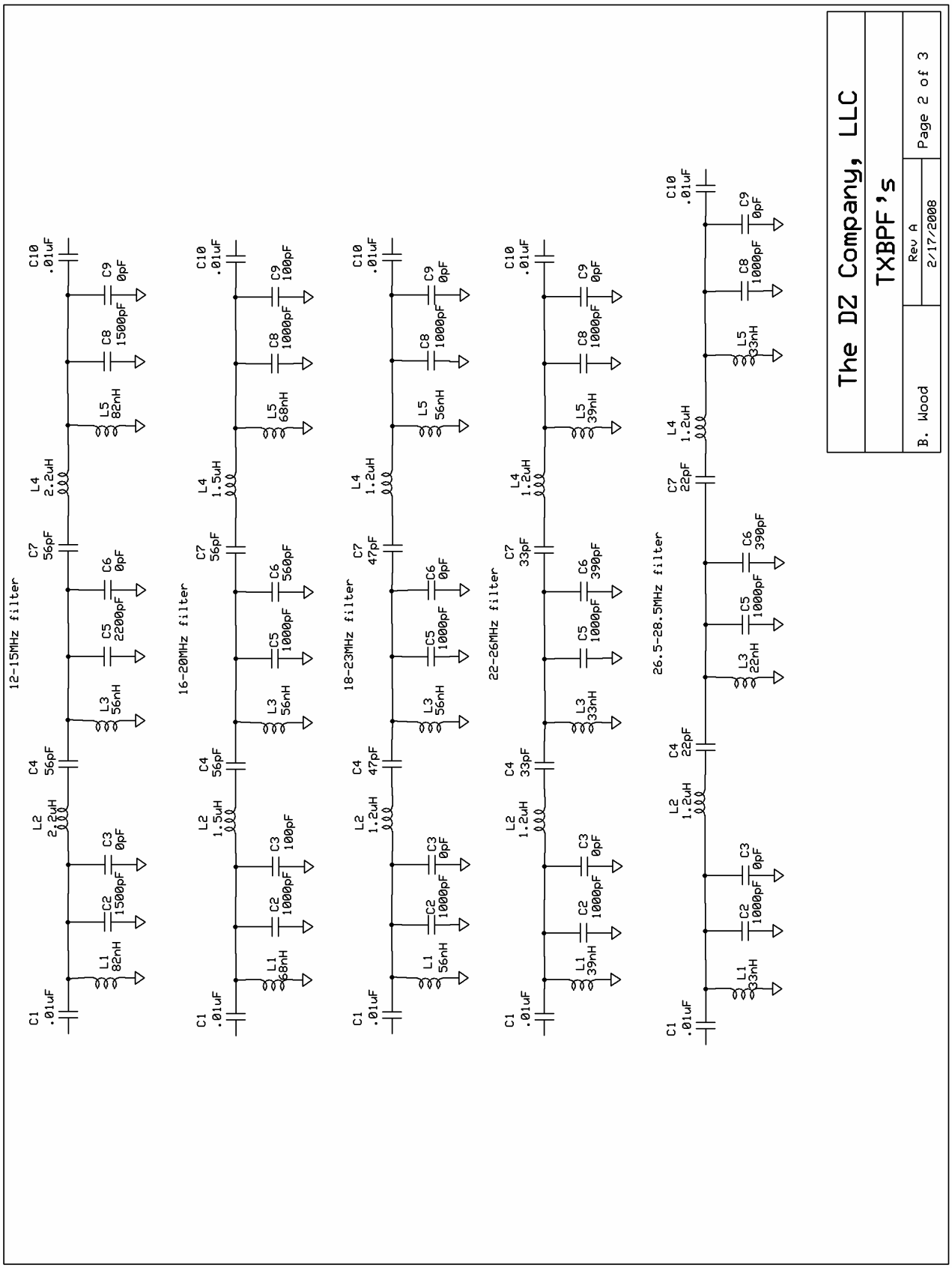
12-15MHz filter
16-20MHz filter
18-23MHz filter
22-26MHz filter
26.5-28.5MHz filter
The DZ Company, LLC
TXBPF's
B. Wood
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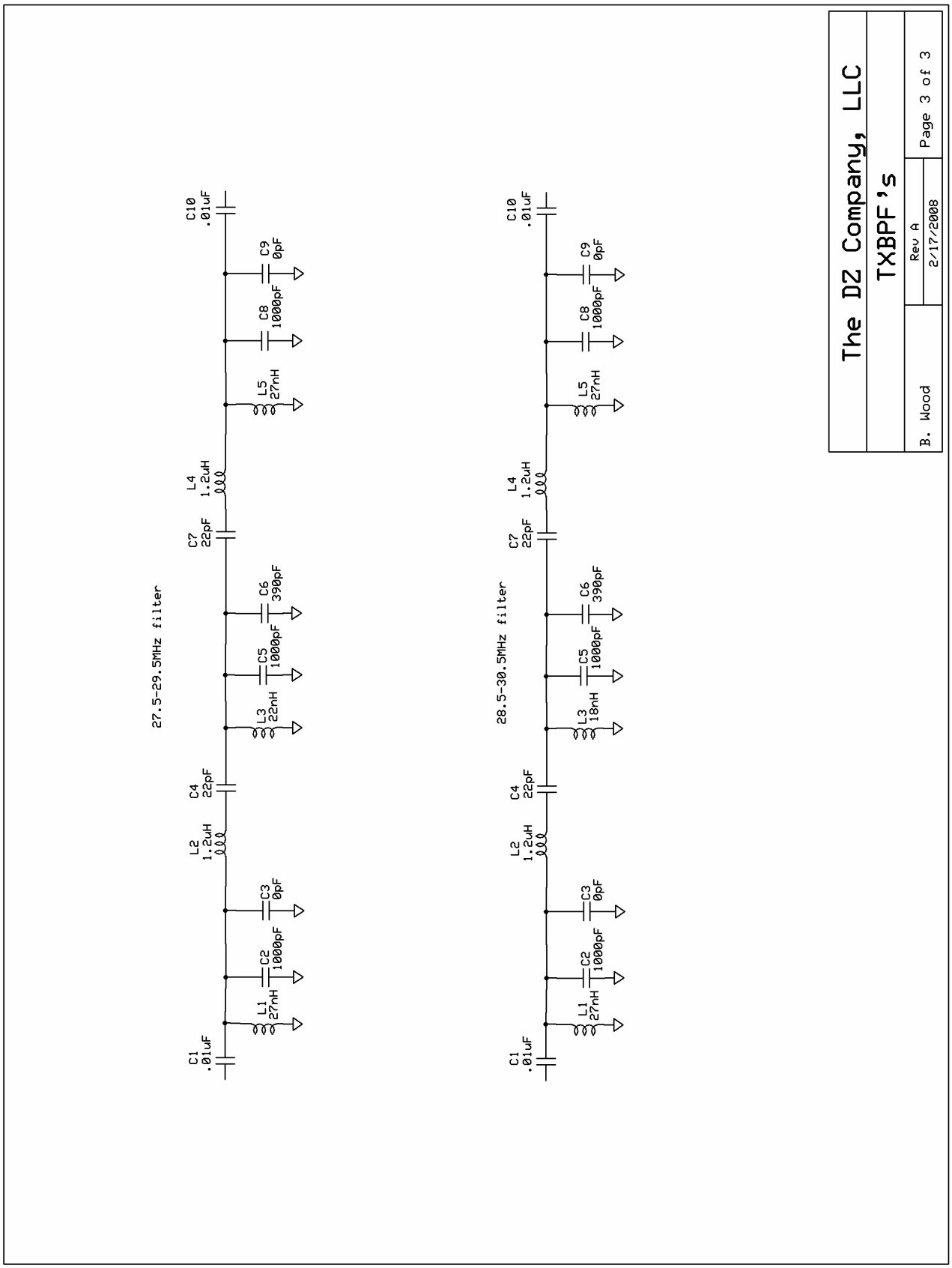
27.5-29.5MHz filter
C1 .01uF
L1 27nH
C2 1000pF
C3 0pF
L2 1.2uH
C4 22pF
L3 22nH
C5 1000pF
C6 390pF
C7 22pF
L4 1.2uH
L5 27nH
C8 1000pF
C9 0pF
C10 .01uF
28.5-30.5MHz filter
C1 .01uF
L1 27nH
C2 1000pF
C3 0pF
L2 1.2uH
C4 22pF
L3 18nH
C5 1000pF
C6 390pF
C7 22pF
L4 1.2uH
L5 27nH
C8 1000pF
C9 0pF
C10 .01uF
The DZ Company, LLC
TXBPF's
B. Wood
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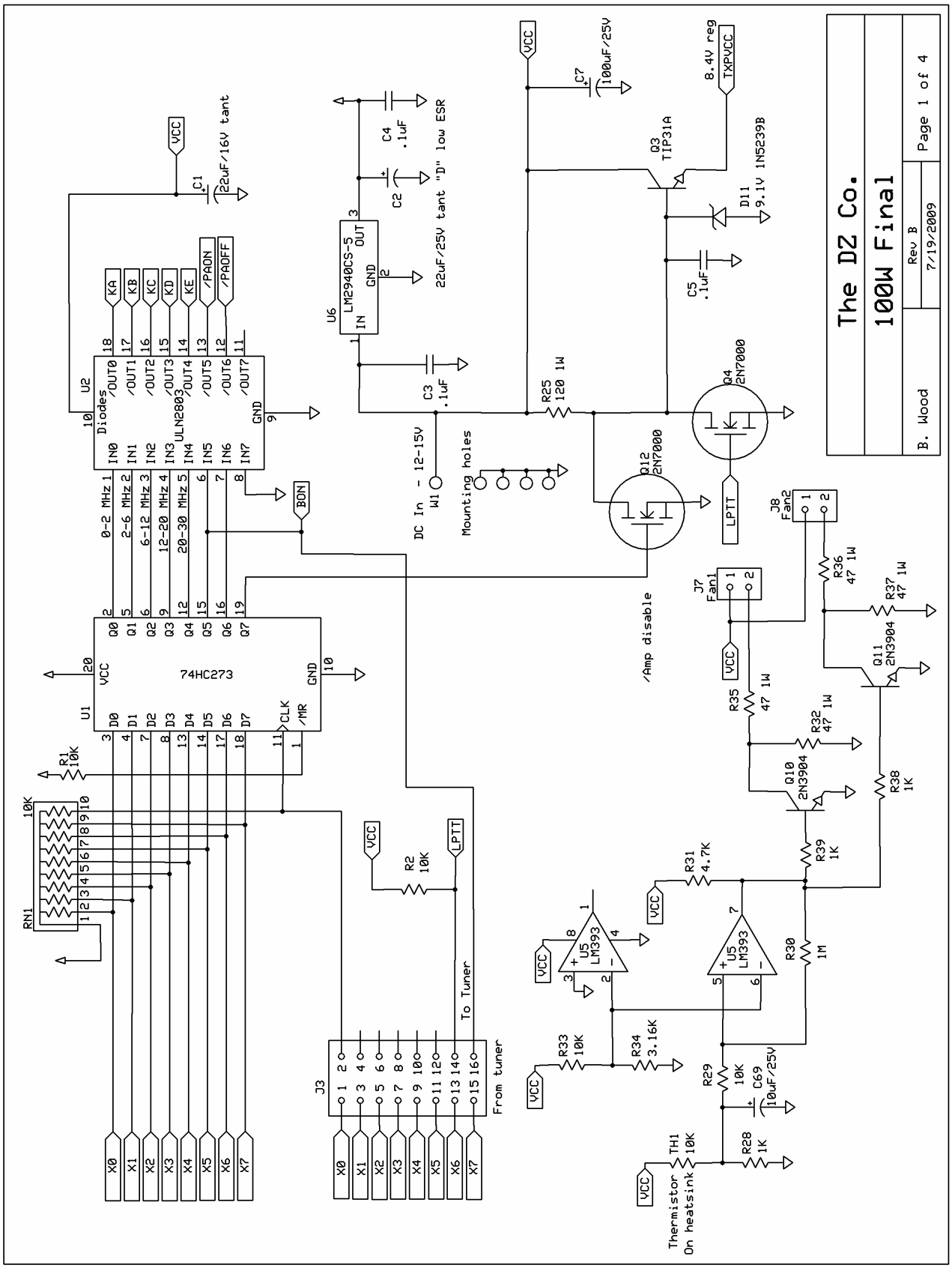
The D2 Co.
100W Final
Rev B
7/19/2009
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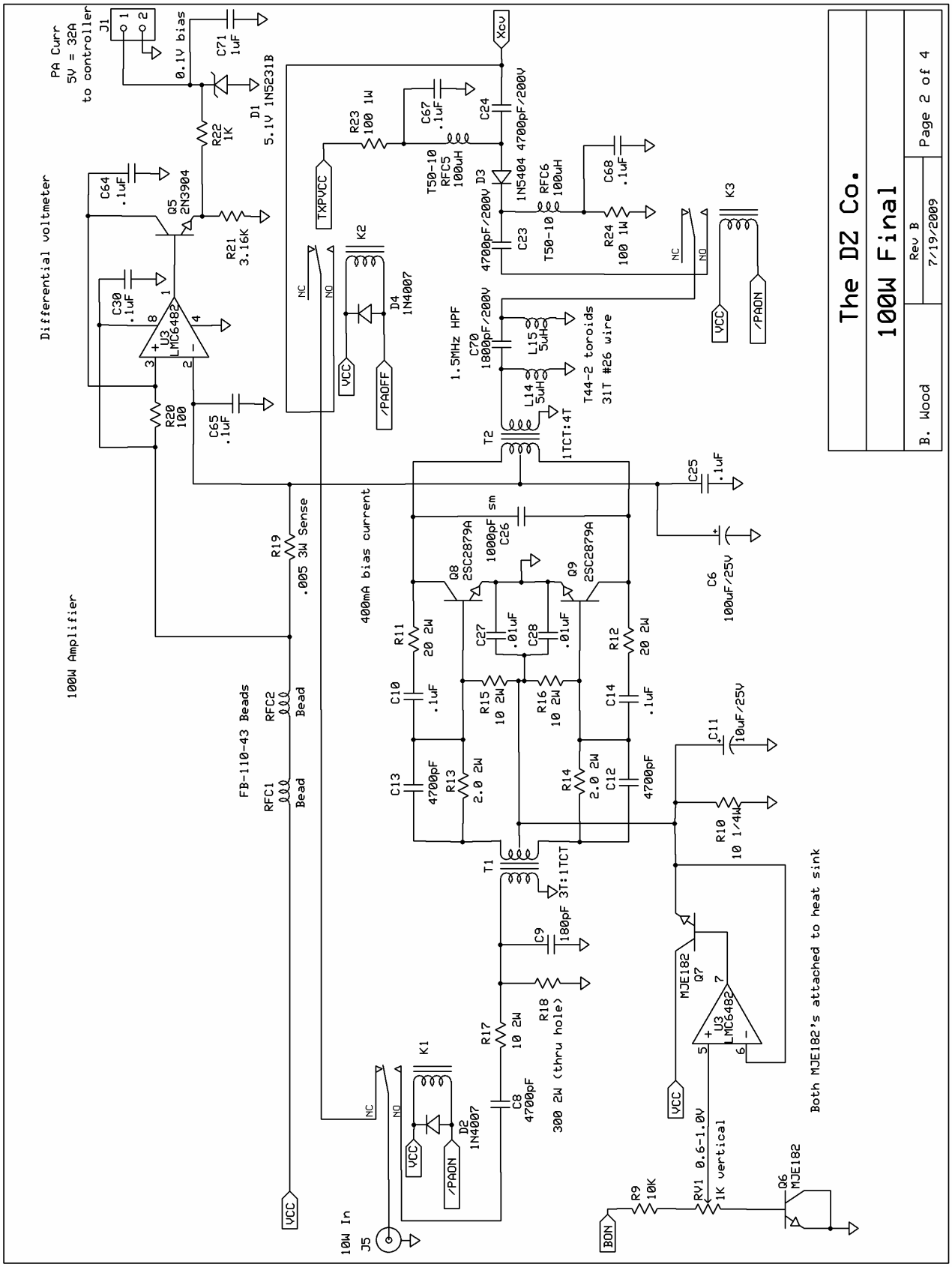
B. Wood
74HC273
ULN2803
LM2940CS-5
LM393
TIP31A
2N7000
2N3904
LPTT
BON
/Amp disable
To Tuner
From tuner
DC In - 12-15V
Mounting holes
Thermistor On heatsink
8.4V reg
9.1V 1N5239B
22uF/16V tant
22uF/25V tant "D" low ESR
100uF/25V
.1uF
10uF/25V
10K
4.7K
3.16K
1K
1M
47 1W
120 1W


The DZ Co.
100W Final
Rev B
7/19/2009
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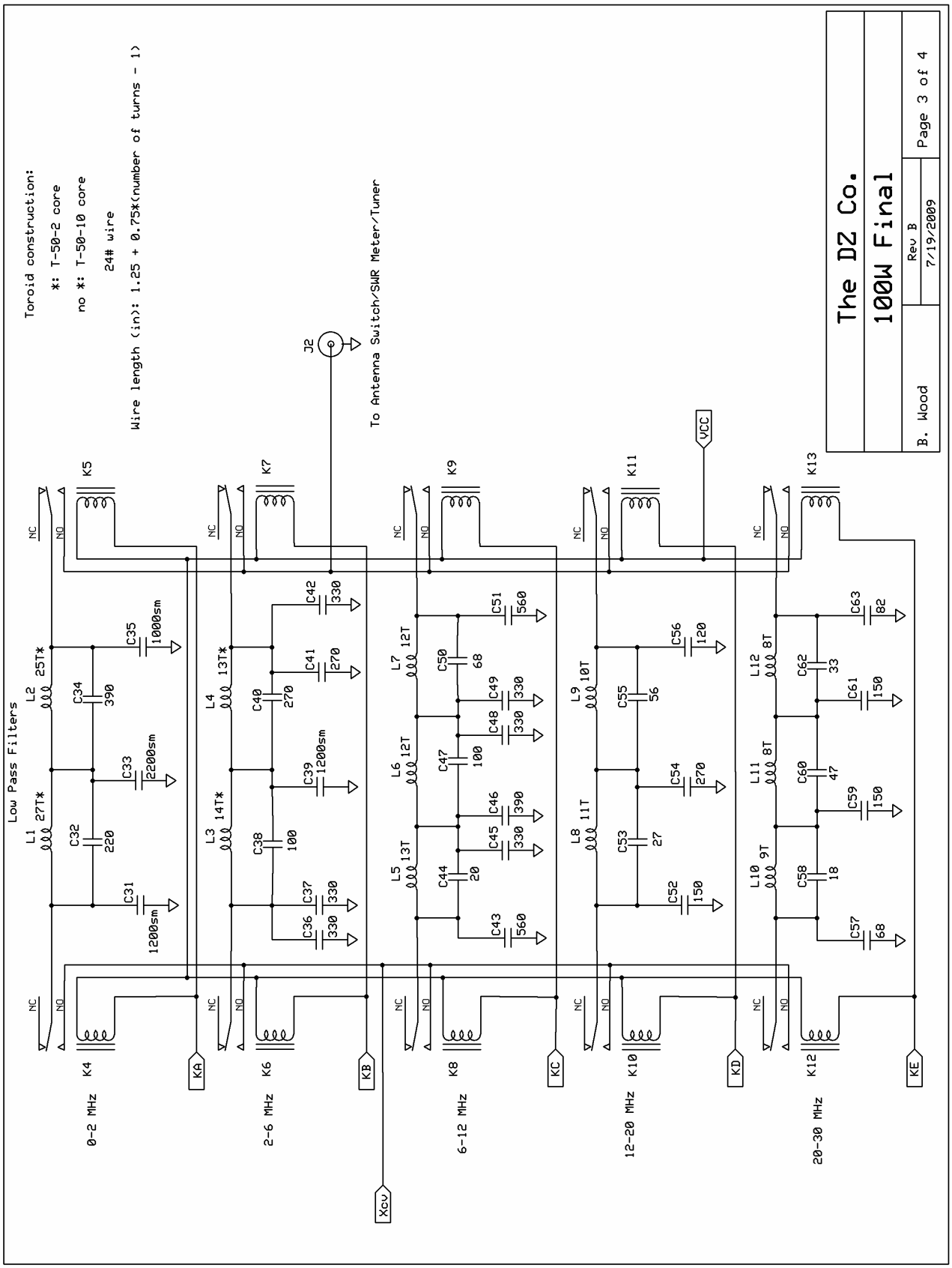
B. Wood
100W Amplifier
Differential voltmeter
PA Curr
5V = 32A
to controller
J1
0.1V bias
C71 1uF
D1 5.1V 1N5231B
R22 1K
Q5 2N3904
C64 .1uF
R21 3.16K
C30 .1uF
U3 LMC6482
R20 100
C65 .1uF
R19 .005 3W Sense
FB-110-43 Beads
RFC1 Bead
RFC2 Bead
VCC
10W In
J5
K1
D2 1N4007
/PAON
C8 4700pF
R17 10 2W
300 2W (thru hole)
R18
C9 180pF
T1 3T:1TCT
C13 4700pF
R13 2.0 2W
C10 .1uF
R15 10 2W
R11 20 2W
Q8 2SC2879A
C27 .01uF
C26 1000pF sm
C28 .01uF
Q9 2SC2879A
R16 10 2W
R12 20 2W
C14 .1uF
C12 4700pF
R14 2.0 2W
400mA bias current
C25 .1uF
C6 100uF/25V
C11 10uF/25V
R10 10 1/4W
Q7 MJE182
U3 LMC6482
RV1 0.6-1.0V
1K vertical
R9 10K
BON
Q6 MJE182
Both MJE182's attached to heat sink
K2
D4 1N4007
/PAOFF
TXPVCC
R23 100 1W
C67 .1uF
T50-10 RFC5 100uH
Xcv
C24 4700pF/200V
D3 1N5404
C23 4700pF/200V
RFC6 100uH
T50-10
C68 .1uF
R24 100 1W
K3
/PAON
1.5MHz HPF
C70 180pF/200V
L15 5uH
L14 5uH
T2 1TCT:4T
T44-2 toroids
31T #26 wire


The DZ Co.
100W Final
B. Wood
Rev B
7/19/2009
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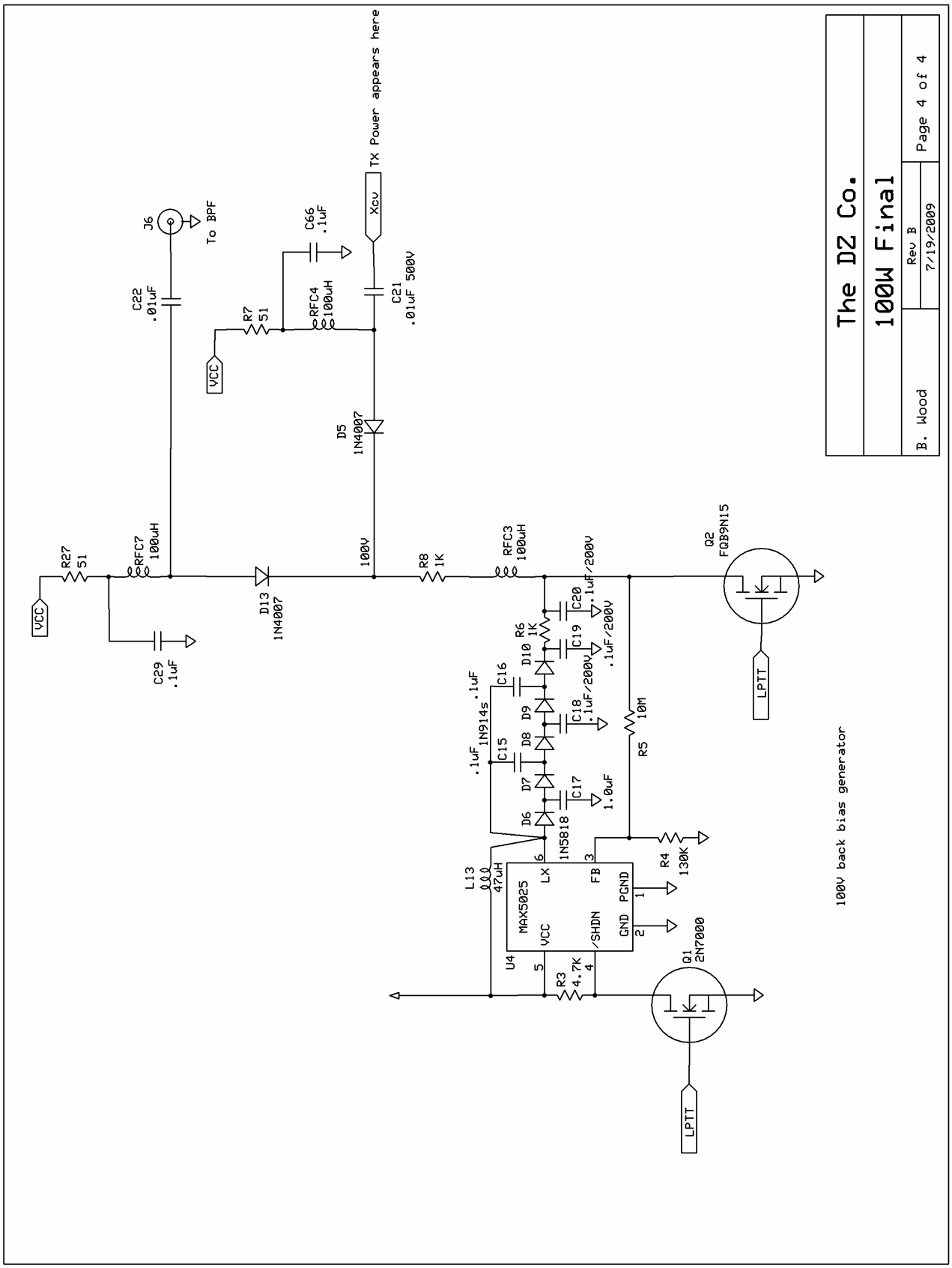
Toroid construction:
*: T-50-2 core
no *: T-50-10 core
24# wire
Wire length (in): 1.25 + 0.75*(number of turns - 1)
Low Pass Filters
0-2 MHz
2-6 MHz
6-12 MHz
12-20 MHz
20-30 MHz
J2
To Antenna Switch/SWR Meter/Tuner
VCC
Xcv
KA
KB
KC
KD
KE
K4
K5
K6
K7
K8
K9
K10
K11
K12
K13
NC
NO
L1 27T*
L2 25T*
L3 14T*
L4 13T*
L5 13T
L6 12T
L7 12T
L8 11T
L9 10T
L10 9T
L11 8T
L12 8T
C31 1200sm
C32 220
C33 2200sm
C34 390
C35 1000sm
C36 330
C37 330
C38 100
C39 1200sm
C40 270
C41 270
C42 330
C43 560
C44 20
C45 330
C46 390
C47 100
C48 330
C49 330
C50 68
C51 560
C52 150
C53 27
C54 270
C55 56
C56 120
C57 68
C58 18
C59 150
C60 47
C61 150
C62 33
C63 82


The DZ Co.
100W Final
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B. Wood
100V back bias generator
J6
To BPF
C22
.01uF
C66
.1uF
Xcv
TX Power appears here
C21
.01uF 500V
R7
51
RFC4
100uH
VCC
D5
1N4007
100V
R27
51
RFC7
100uH
D13
1N4007
R8
1K
RFC3
100uH
C20
.1uF/200V
C19
.1uF/200V
C18
.1uF/200V
C29
.1uF
R6
1K
D10
D9
D8
D7
D6
C16
.1uF
C15
.1uF
C17
1.0uF
1N914s
1N5818
R5
10M
R4
130K
L13
47uH
U4
MAX5025
VCC
LX
FB
/SHDN
GND
PGND
R3
4.7K
Q1
2N7000
Q2
FQB9N15
LPTT
LPTT